Barrel Drift Tubes Trigger Electronics Review

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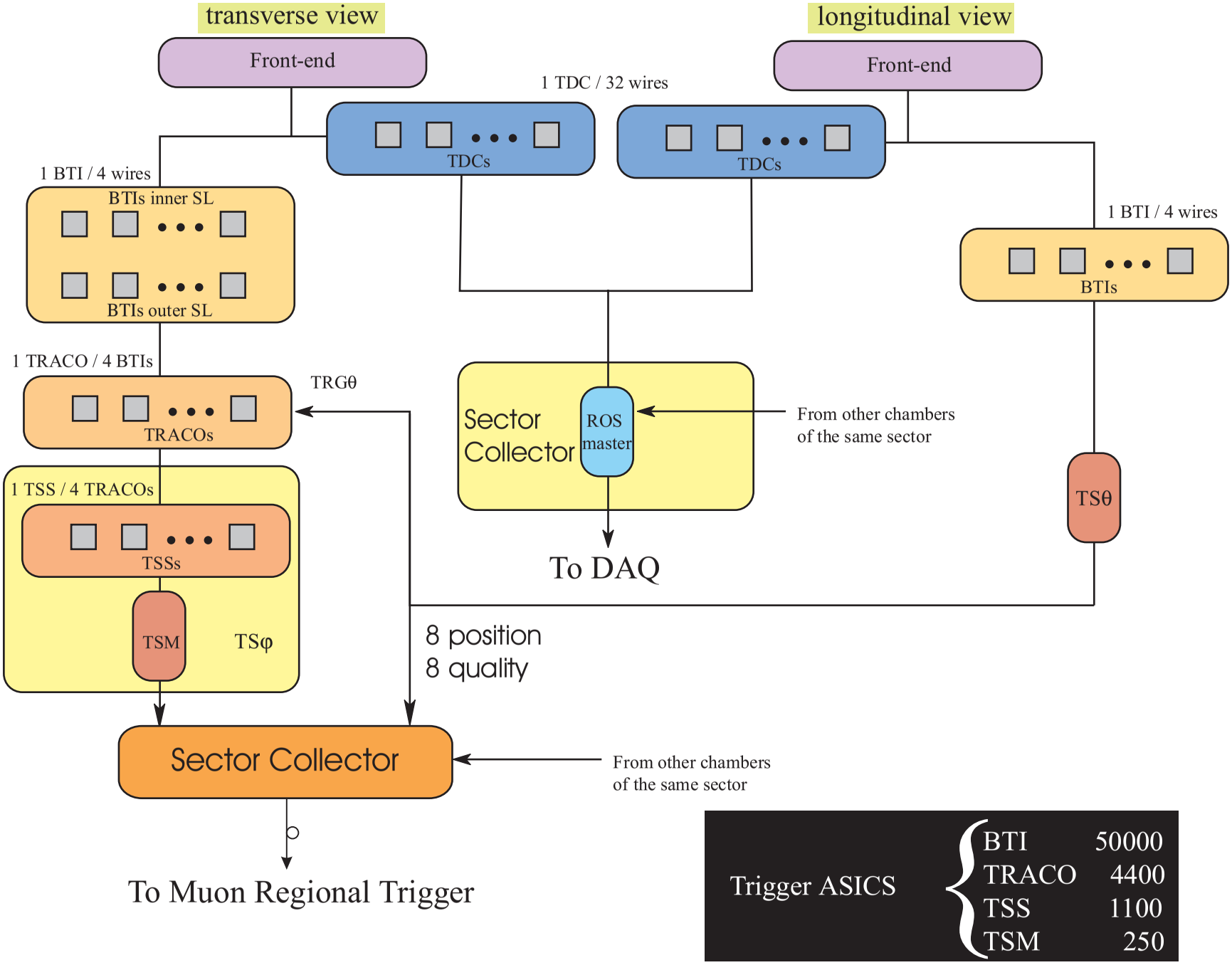
I.N.F.N. Sezione di Padova, ITALY

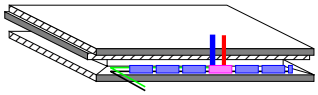
CERN november 15, 1999

Overview of the electronics layout of a chamber

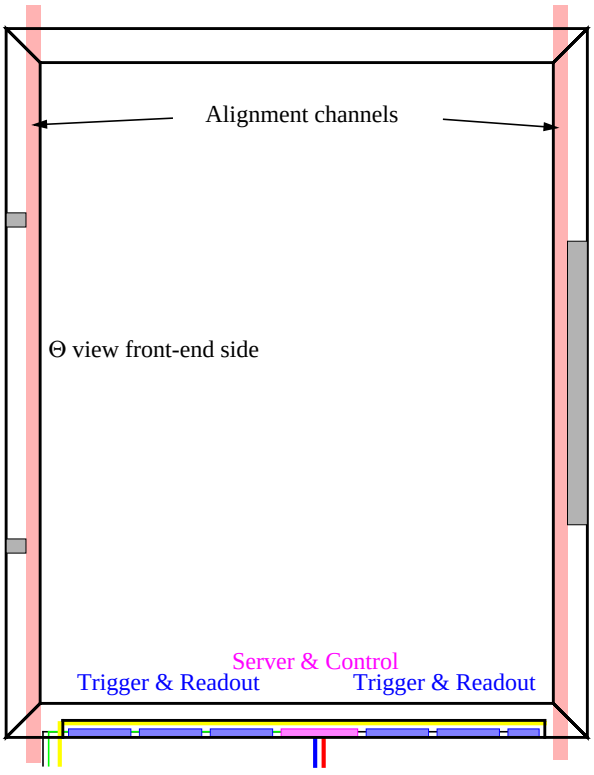


CHAMBER ELECTRONICS LAYOUT

ELv15st: Padova, 2 nov 1998



Cooling pipes
LV power
Slow controls
Fast alarming
Trigger & Readout links



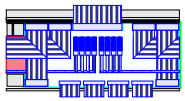
Φ view front-end side

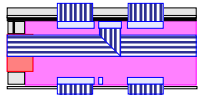
MB1 Chamber plan sketch

Chamber Trigger and Readout electronics is lodged in a mini-crate fixed in the front-end side of the C-profile.

The electronics consists of 128 channels Trigger and Readout boards sandwitched together: two units are needed for the θ side and three units plus a small 32 channel unit are used for the ϕ view

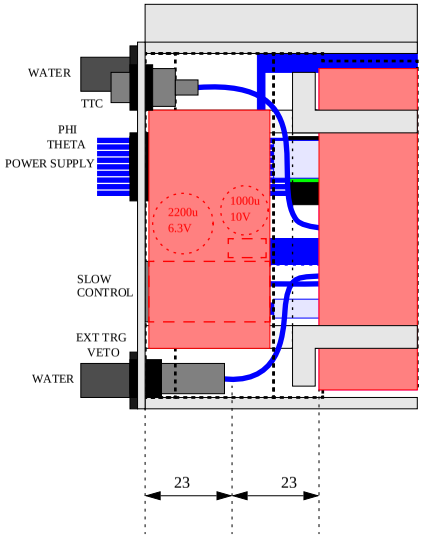
One Server and Control performing data collection/transmission and local controls is located in the middle.



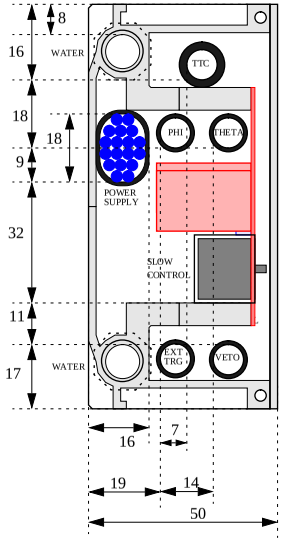


Chamber Electronics Box

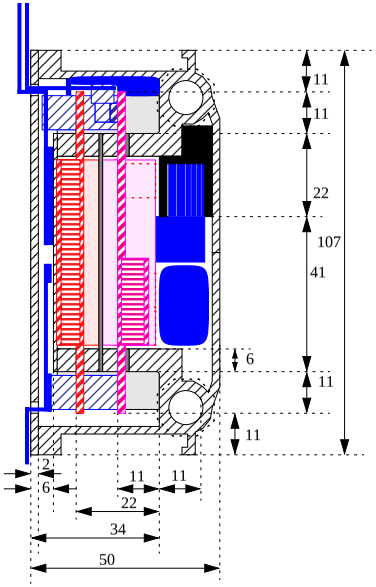
BOXv10, Padova 2 nov 1998



IO side:
Power supply decoupling board
Power supply cable outlet
Water connections
TTC, Trigger sync IOs, Slow Control



Box section:
Panel IOs

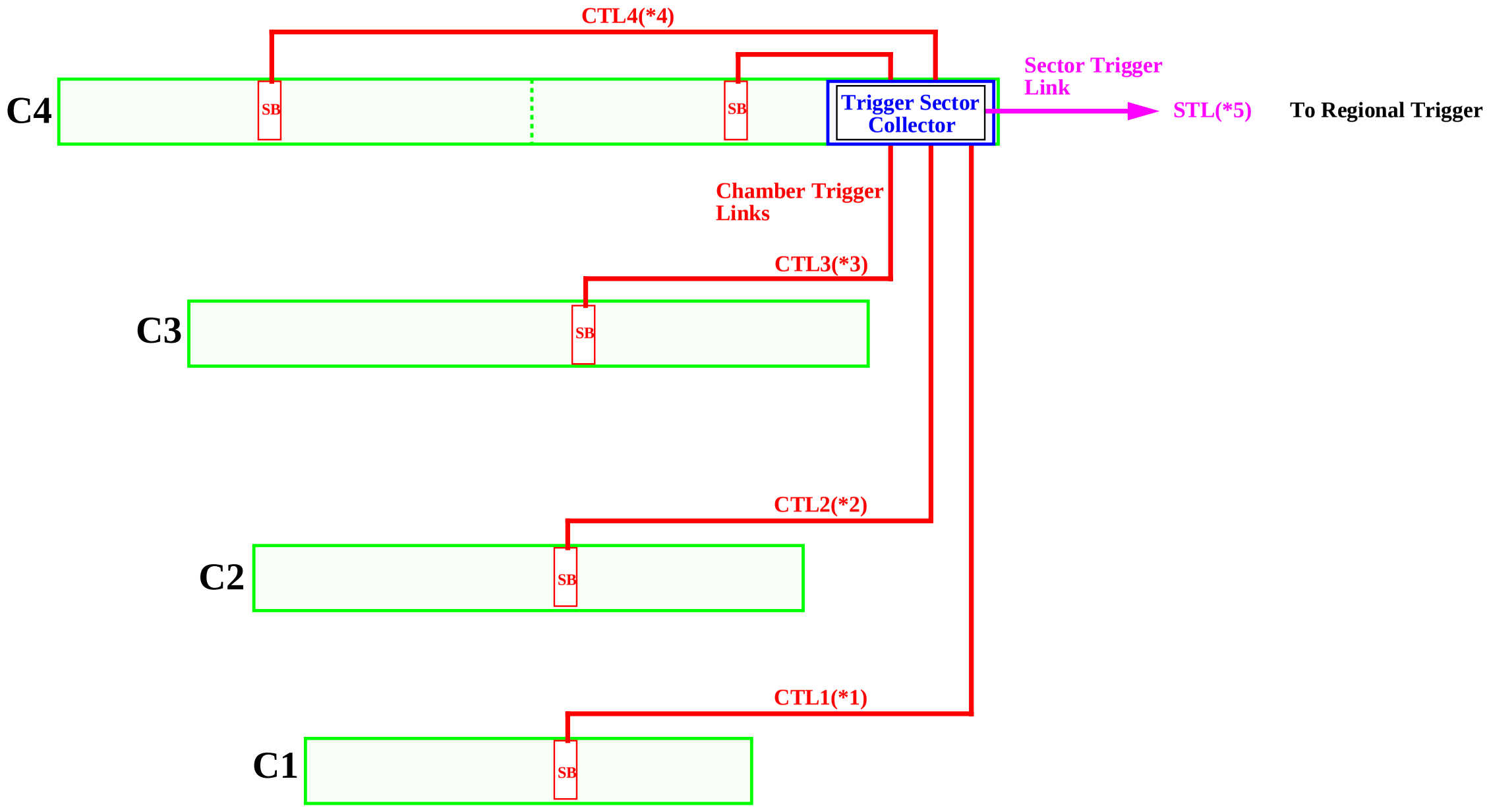


Electronics section:
Trigger and Readout boards
Internal cabling
Cooling system

CHAMBER TRIGGER LINKS: system interconnections

CTL1v12: Padova, 14 nov 1999

SB: Server Board
SU: Sorting Unit
TTX: Trigger Transmitter



(*1) Station 1 Trigger Link

Φ(0:11) Radial of track
Φb(0:9) Bending of track
Q(0:2) Quality of track
Ist/IInd Track strobe
OVLP Overlap flag
CNT Control flag
Θ(0:15) Theta SL hits (8+8)

40 wires shielded flat cable

(*2) Station 2 Trigger Link

Φ(0:11) Radial of track
Φb(0:9) Bending of track
Q(0:2) Quality of track
Ist/IInd Track strobe
OVLP Overlap flag
CNT Control flag
Θ(0:15) Theta SL hits (8+8)

40 wires shielded flat cable

(*3) Station 3 Trigger Link

Φ(0:11) Radial of track

Q(0:2) Quality of track
Ist/IInd Track strobe
OVLP Overlap flag
CNT Control flag
Θ(0:15) Theta SL hits (8+8)

40 wires shielded flat cable

(*4) Station 4 Trigger Link

Φ(0:11) Radial of track
Φb(0:9) Bending of track
Q(0:2) Quality of track
Ist/IInd Track strobe
OVLP Overlap flag
CNT Control flag

40 wires shielded flat cable

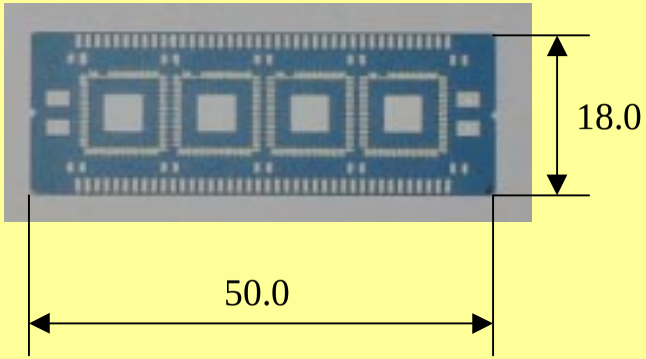
(*5) Sector Trigger Link

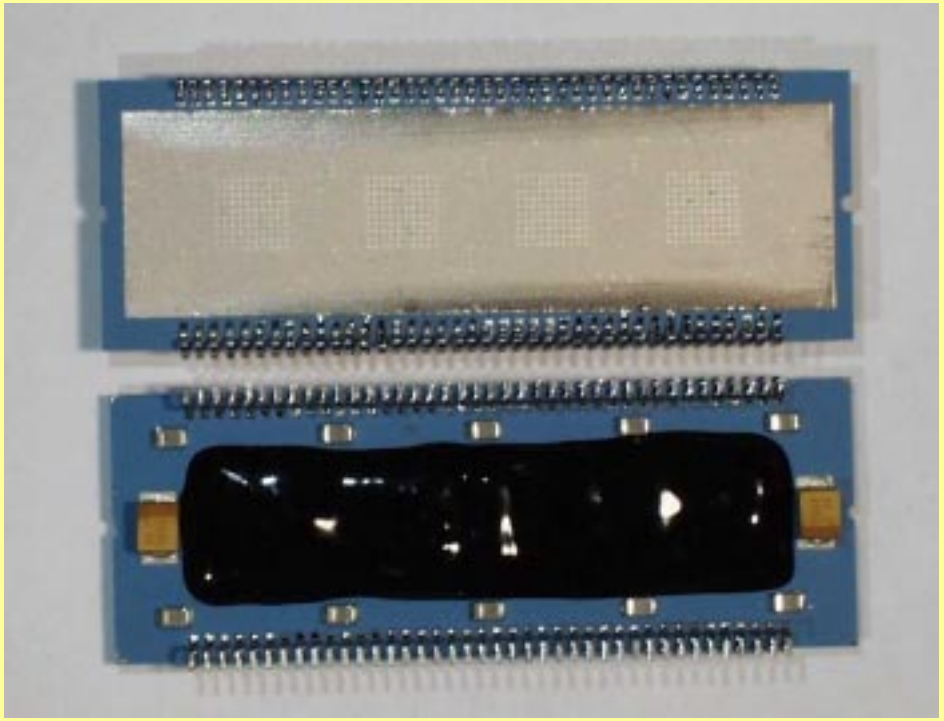
147 bits Trigger Data

12 fibers ribbon cable

BTI Multichip Module

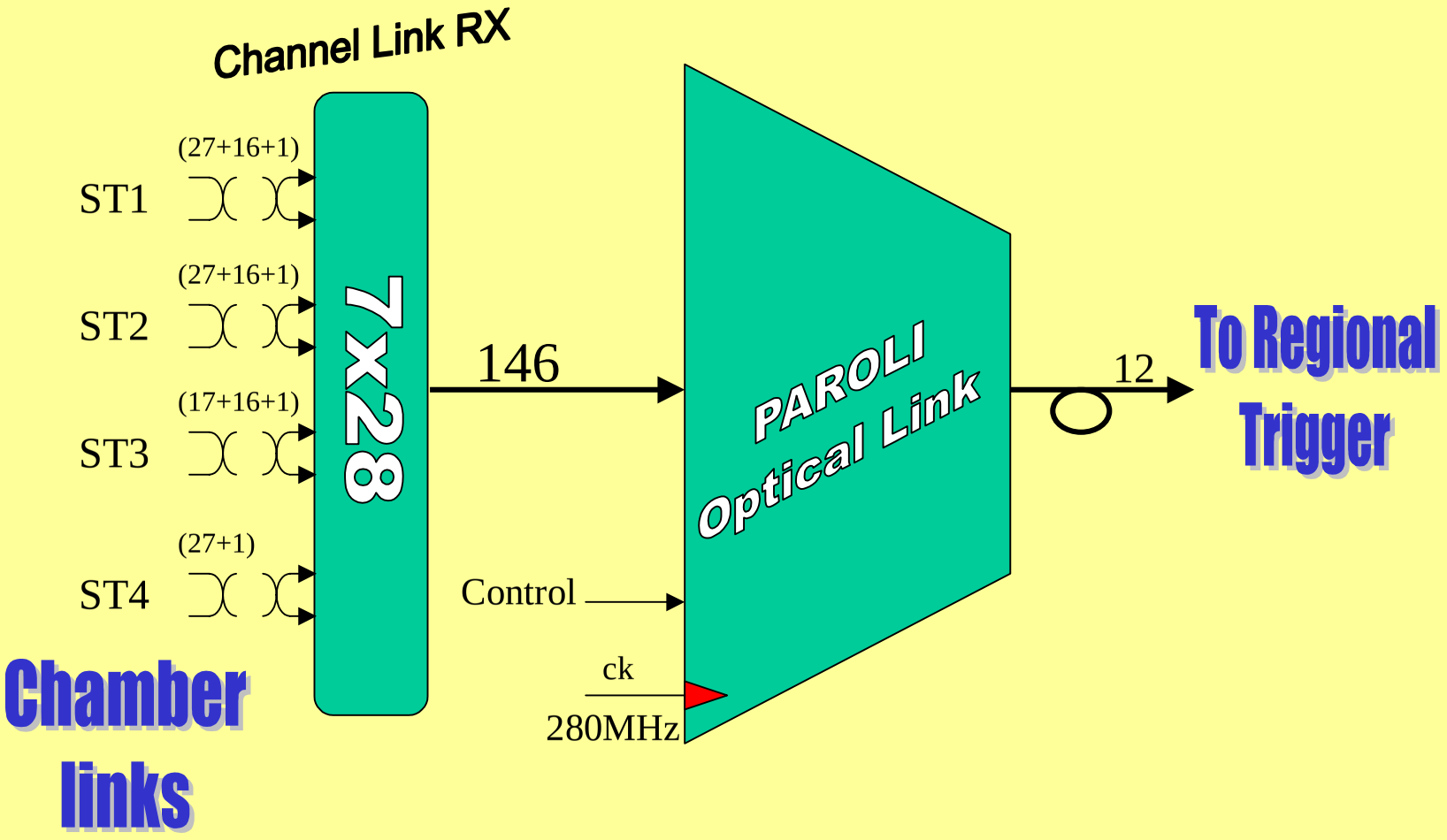
LTCC substrate - 07/99



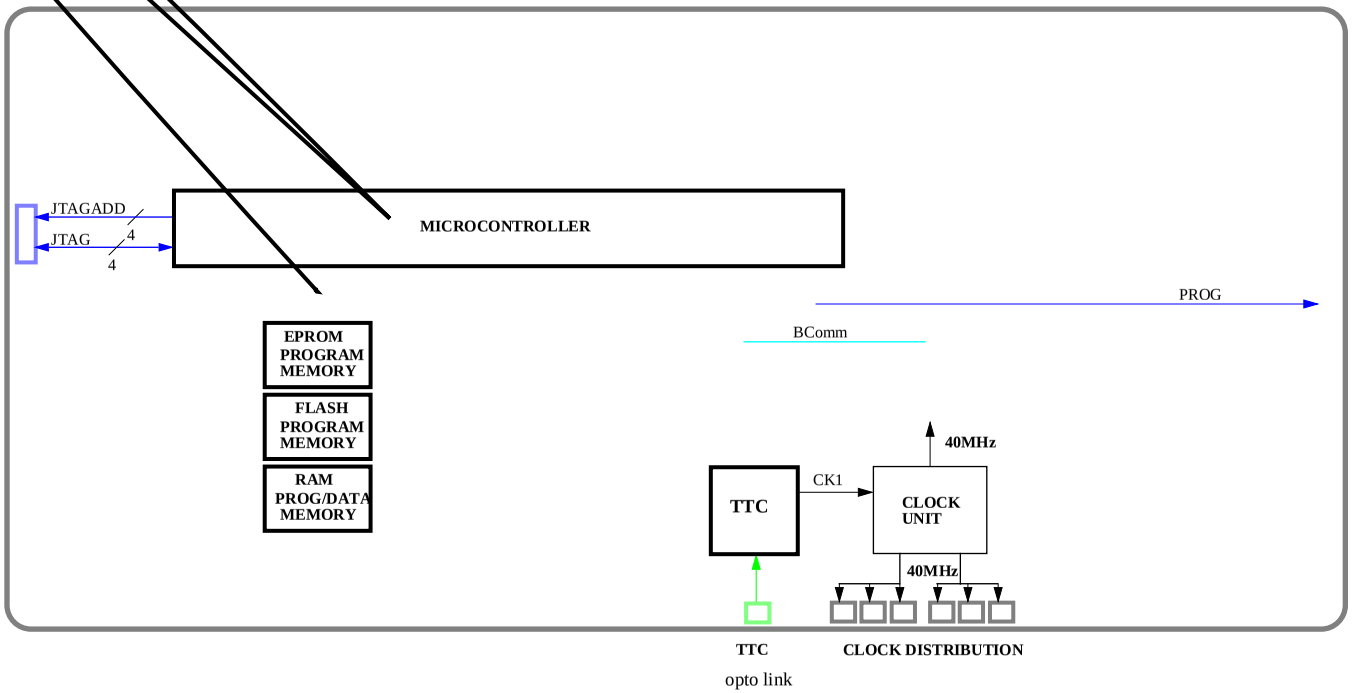


Sector Collector - Trigger electronics

Trigger Optical Link

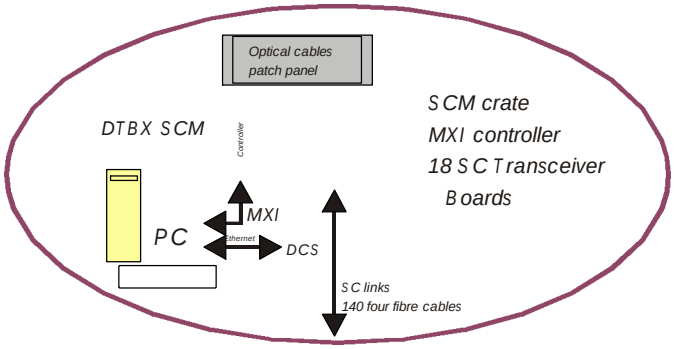


CHAMBER CONTROL BOARD

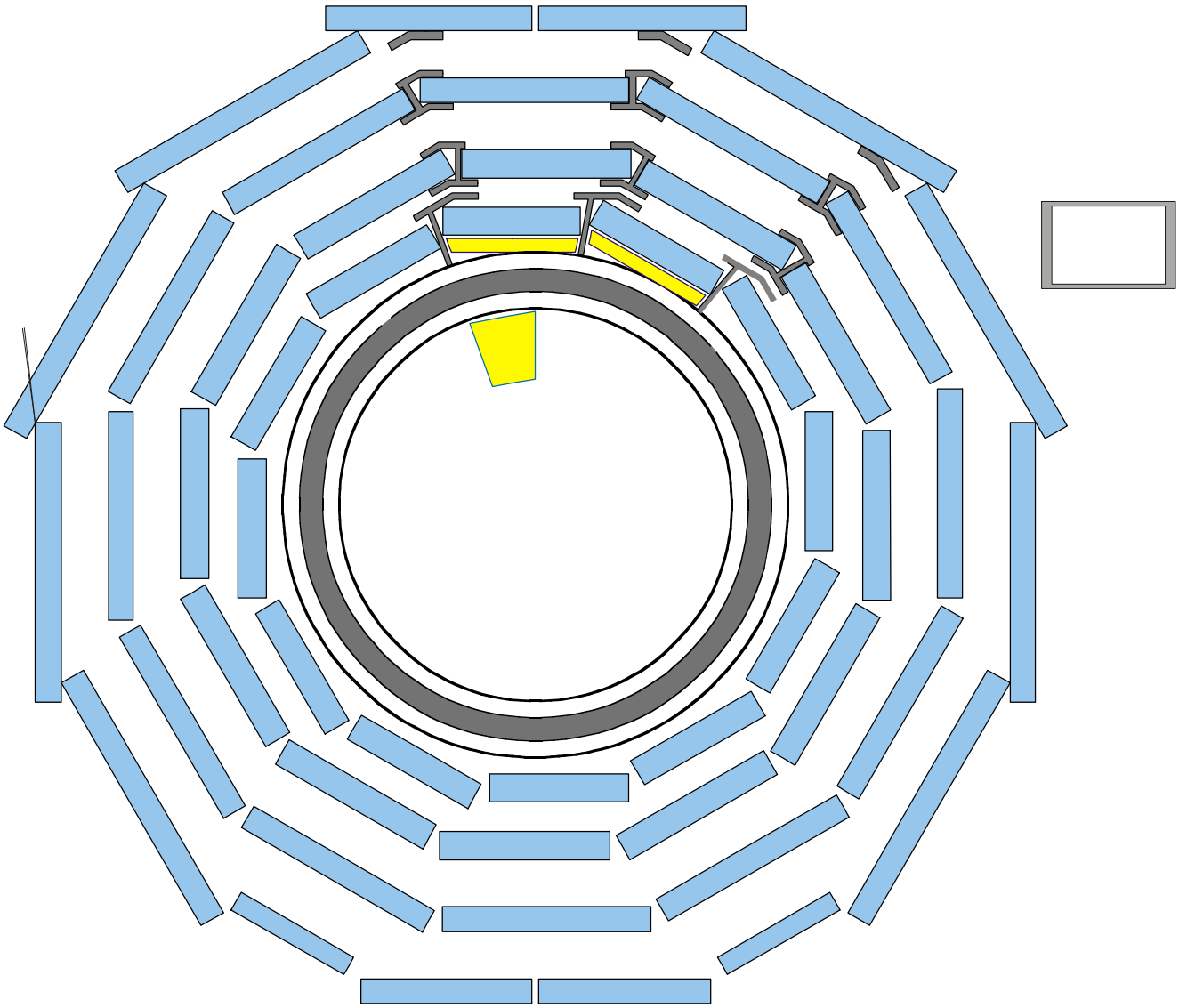


DTBX SLOW CONTROL LAYOUT

Padova, october 21th, 1999



DTBX
SC electronics
in Control Room



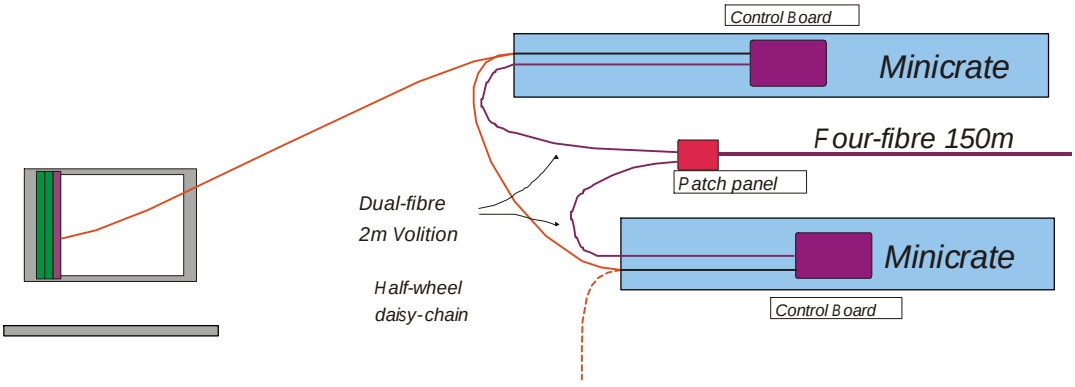
MARTINELLI ROBERTO

DTBX SLOW CONTROL LAYOUT

Padova, october 21th, 1999

DTBX
SC electronics
in Control Room

SC links
140 four-fibre cables
10 from Sector CB
130 from Chambe CB



Padova

STATUS OF BMUON CHAMBERS TRIGGER AND CONTROL ELECTRONICS

Chamber Trigger ASICS:

Four ASICS have been designed to fullfill chamber trigger requirements:

1. BX identification & wide angular acceptance — BTI
2. Angle and position measurement of tracks — BTI+ TRACO
3. Track sorting on bending angle — TRACO+TSS+TSM
4. Noise rejection — TRACO+TSS+TSM

- BTI Bunch and Track Identifier

full performance chip	DONE
5 tested prototypes in PLCC68 ceramic package	TESTED
200 tested pcs in TQFP64 plastic package	TESTED
200 tested dies	ARRIVED
functional tests with beam and cosmic rays	DONE
54000 kgd (tender+production)	6/00-12/01 (1y)

- BTIM BTI multichip module

Ist prototype: 4 BTIs in plastic package 66mm x 24mm	
on FR4 substrate 100pins SMT type; 25 pcs	DONE
irradiation tests in gamma cell 5krad and 10krad	DONE
irradiation tests with thermal and fast neutrons	DONE
II prototype: 4 BTI dies on LTCC substrate 50x18 mm^2	
80pins SMT type, full performance; 40 pcs	ARRIVED
test with simulated tracks	12/99
Steady-State Life test (2000h at 125°C)	
MIL-STD-883E Method 1005.8	3/00
irradiation tests	10/99-7/00
12000 pcs (tender+production)	9/00-3/03 (2y)

BTI functionality has been fully tested with very good results. For a definitive approval, tests on a fully assembled Trigger Board are planned, in order to check BTI-TRACO interface.

- TRACO Track Correlator

full performance chip	DONE
50 tested prototypes in QFP240 plastic package	ARRIVED
functional tests	12/99-3/00
full performance chip IInd submission	6/00 !!
50 tested prototypes in QFP240 plastic package	9/00
5100 tested pcs in QFP240 (tender+production)	1-12/01 (1y)

ATMEL has validated TRACO prototypes, using the supplied test vectors, getting a different output wrt simulations. The result, the same for all prototypes, didn't change using different clock frequencies and applying skews to TRACO inputs.

Examining chip schematics, no errors have been discovered so far. In the layout, done by an ATMEL engeneer, a problem has been discovered in the routing of clock nets; but it has to be confirmed.

If laboratory tests, expected to start in december, will confirm the validation results, a new set of prototypes with a corrected layout has to be done. If this would be the case we hope to take advantage of Trigger Board tests to discover other potential problems and/or possible improvements and to produce a new TRACO schematic.

- TS TSS: Track Sorter Slave

full performance chip but 5V technology	DONE
10 TSS prototypes in CQFP ceramic package	ARRIVED
full performance prototype submission	6/00
10 tested pcs	9/00
2000 tested pcs (tender+production)	1-12/01 (1y)

TSM: Track Sorter Master

Ist prototype	3/00
IInd, full performance prototype submission	6/00
10 tested pcs	9/00
2000 tested pcs (tender+production)	1-12/01

TSS prototypes, whose functionality have been verified in the laboratory, will be tested on the Trigger Board prototype.

Chamber Trigger PCBs:

Chamber electronics is lodged in minicrates and segmented in 128 channel units consisting in a Readout Board and a Trigger Board sandwitched together.
A small 32 channels unit is necessary to mach the number of channels of stations 1 and 4. A Server Board, lodged in the central part of the minicrate, accomplishes track sorting tasks (TSM) and trigger data transmission to the Sector Collector Unit.

- **PHITRB128**	<u>128 channels phi view Trigger Board</u>	
	full performance but 5V/3.3V mixed power supply	
	to use present version of TSS	DONE
	test with simulated tracks	12/99-3/00
	test on DTBX chamber	3-9/00
	irradiation and reliability tests	4-12/00
	1000 pcs (tender+production)	3/01-9/03 (2y)
- **PHITRB32**	<u>32 channels phi view Trigger Board</u>	
	full performance	3/00
	test with simulated tracks	6/00
	test on DTBX	6-12/00
	irradiation and reliability tests	9-12/00
	90 pcs (tender+production)	3/01-3/02 (6m)
- **THETATRB**	<u>128 channels theta side Trigger Board</u>	
	full performance	3/00
	test on DTBX	6-12/00
	irradiation and reliability tests	9-12/00
	350 pcs (tender+production)	3/01-9/03 (2y)
- **SB**	<u>Server Board</u>	
	Ist prototype (needed for tests of ASICS and	
	PCB prototypes)	3/00
	IInd prototype: full performance board	6/00
	test on DTBX	9-12/00
	irradiation and reliability tests	9-12/00
	240 pcs (tender+production)	3/01-9/02 (1y)

Chamber Control PCBs:

Inside chamber minicrate a Control Unit (sandwitched to the Server Board) takes care of controls and monitoring functions:

- Configuration of chamber electronics via JTAG bus with PCB individual addressing
- TTCrx interfacing
- Clock and timing signals distribution
- Control of I^2C busses for Front-End and Alignment
- Test pulse generation and distribution:
    - Front-End threshold scanning
    - TDC offset measurement
    - Chamber electronics diagnostics
- Temperature monitoring (sensors in Front-Ends, Readout and Trigger PCBs and on chamber surface)
- Gas pressure measurement (to be evaluated)
- Low Voltage monitoring for Front-Ends and chamber electronics
- Power-on sequencing and control of chamber electronics
- Slow Control interface via two (optical and electrical) RS232 interfaces
- Chamber electronics Built-In-Self-Test and diagnostics
- Possibility of remote program downloading

We are investigating the possibility to design a single PCB with both Server and Control functions.

- CB	Control Board	
	Ist prototype (BTI tests)	DONE
	IInd prototype (irradiation tests)	DONE
	irradiation tests (neutrons)	5-12/99
	full performance board	6/00
	test on DTBX	9-12/00
	irradiation and reliability tests	9-12/00
	260 pcs (tender+production)	1/01-6/02 (1y)

Sector Trigger PCBs:

A Sector Collector unit, lodged in the fourth station minicrate takes care of trigger data transmission to Control Room via fast optical links.

We are evaluating the possibility to move it out of detector, on the balconies.

- SCB	Sector Collector Board	
	Ist prototype of Trigger optical link (PAROLI)	DONE
	IInd prototype of Trigger optical link (VCSELs)	3/00
	full performance board	6/00
	test on DTBX	9-12/00
	irradiation and reliability tests	9-12/00
	65 pcs (tender+production)	6/01-12/02

PAROLI (Siemens) Sector Trigger Link characteristics:

- transmission of 147 @ 40MHz => 6 Gbit/s
- Maximum power dissipation: 5 W
- Cost: 1.6 kSF

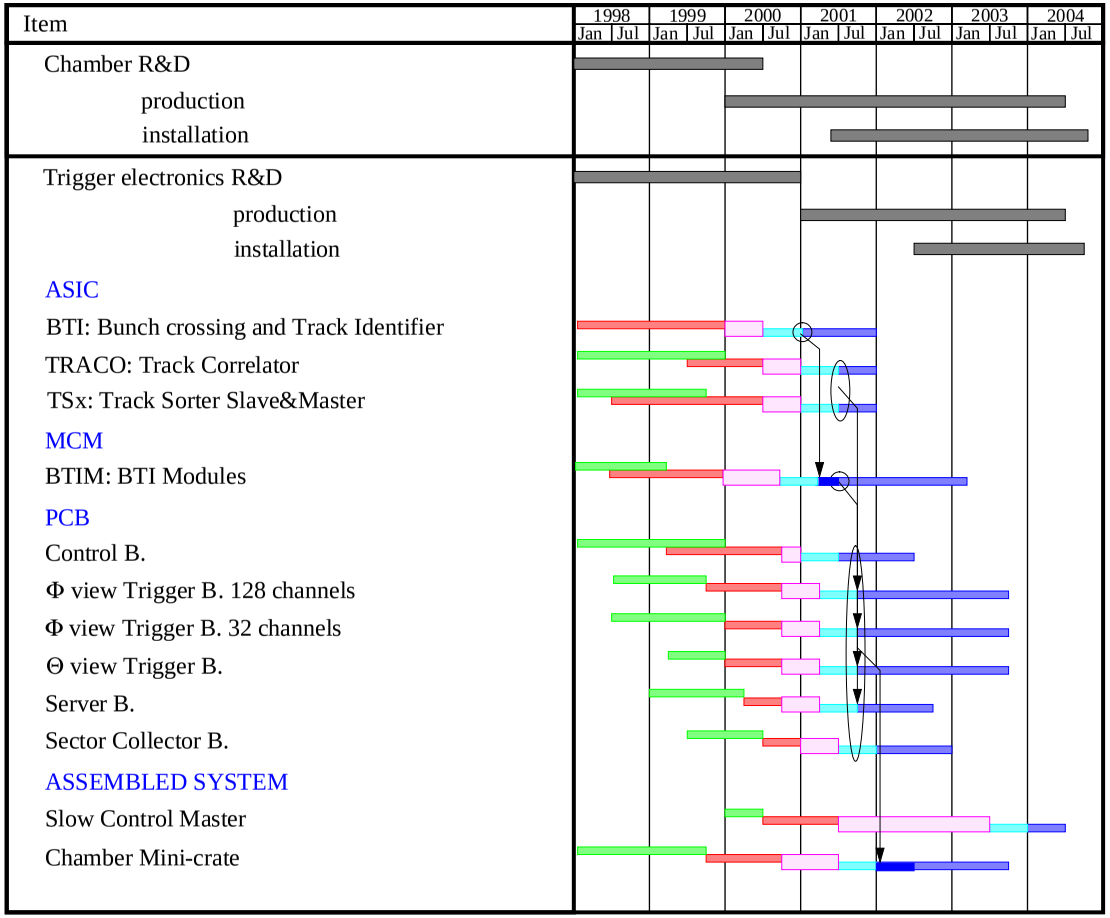
In case we should find a reasonable technical solution to move Sector Collector electronics on the balconies we could use a VCSEL array (Honeywell) to replace the PAROLI transceiver. This solution would be cheaper, flexible and more reliable.

Detector Control PCBs:

Chambers are individually connected via an optical RS232 to a transceiver module (SCR) lodged in a dedicated VME crate in Control Room; 16 chambers are connected to each module. The DTBX detector control is accomplished by a PC controlling the SCR crate with MXI bus.

- SCR	<u>Slow Control Receiver</u>	
	full performance board	6/00
	test on DTBX	9-12/00
	20 pcs (tender+production)	6/03-6/04 (6m)

Schedule of Chamber Trigger and Control Electronics



august 27, 1999

planning

test&prototypes

tender+prod/test