

BTI Status

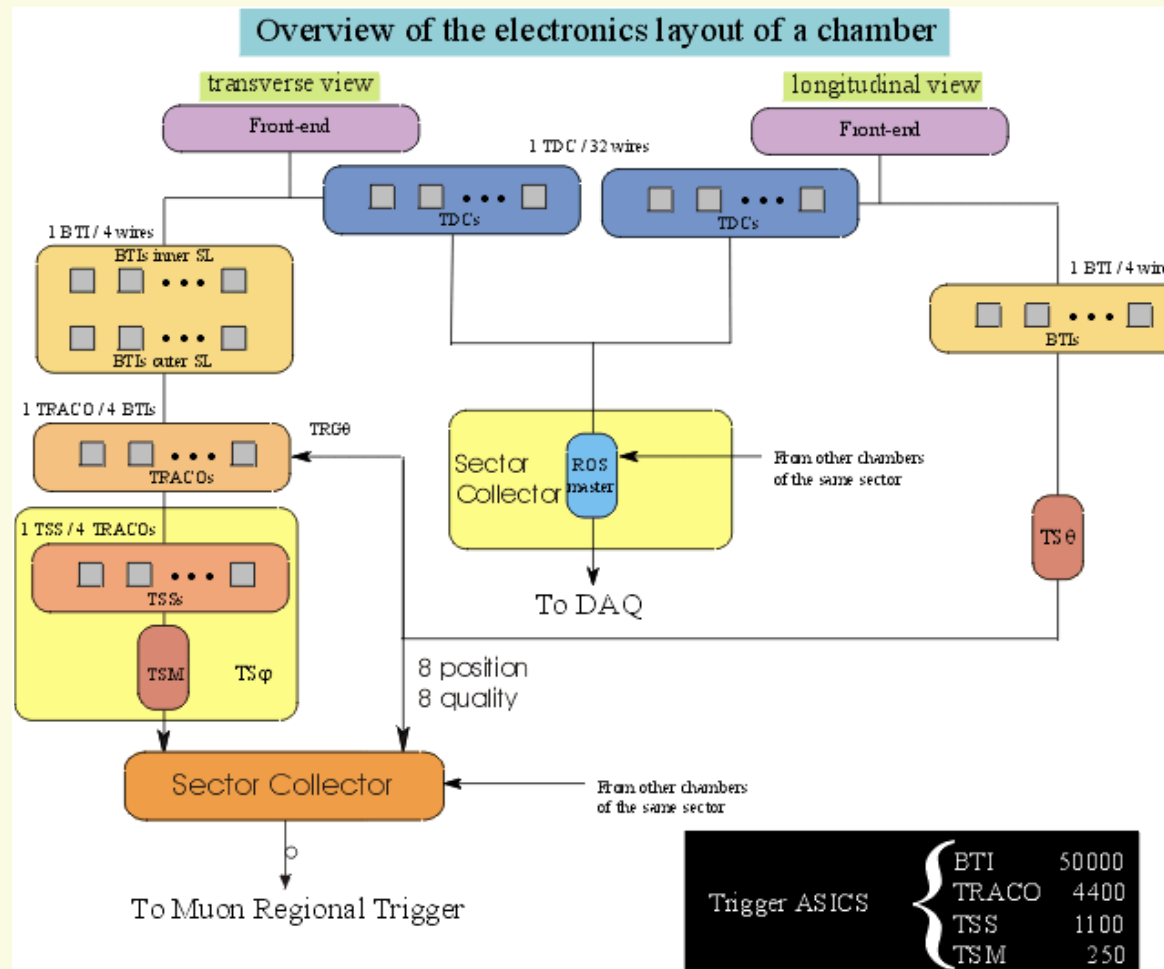
R. Martinelli

I.N.F.N.

Sezione di Padova

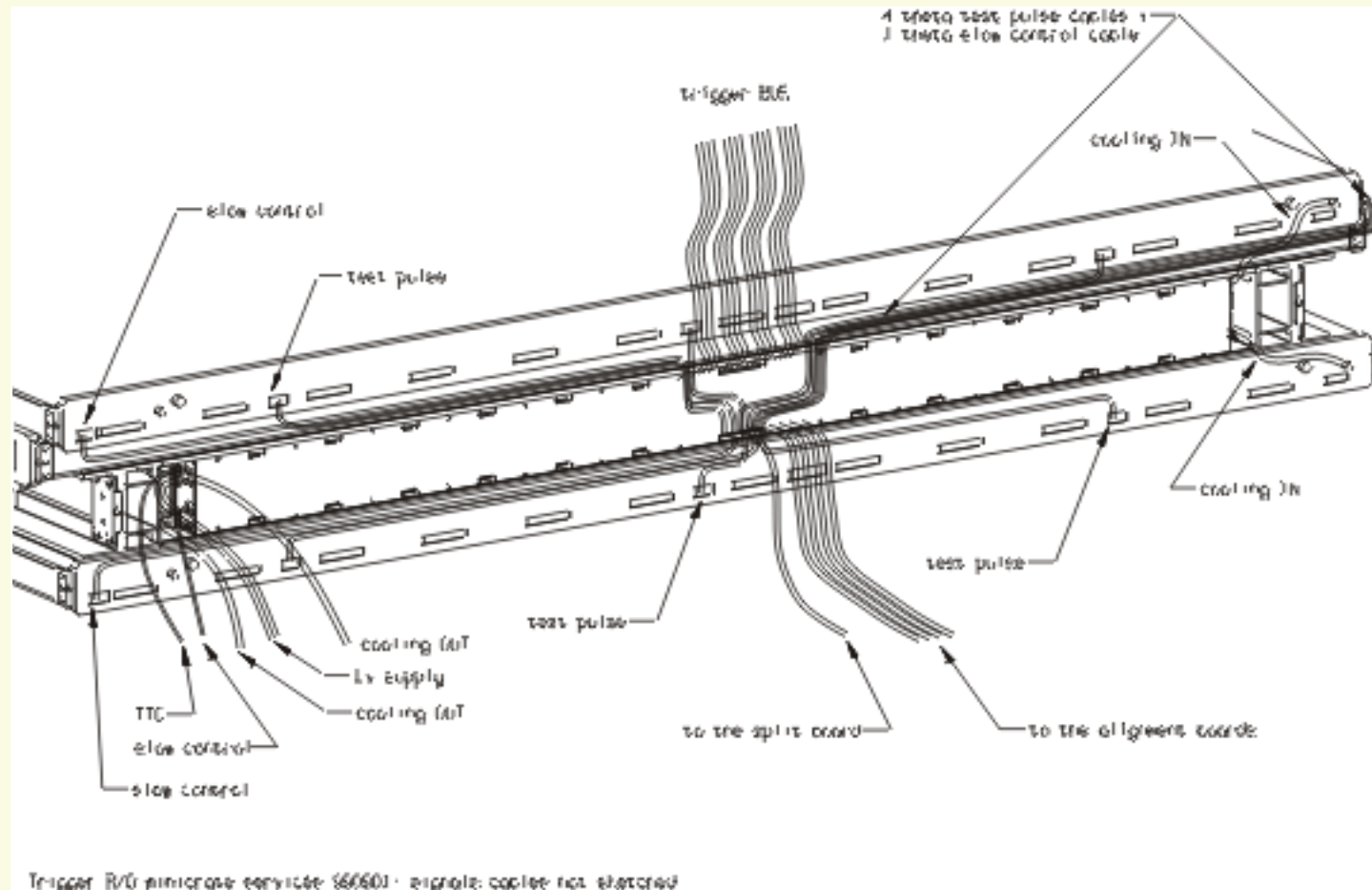
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DT Chamber Electronics Block Scheme



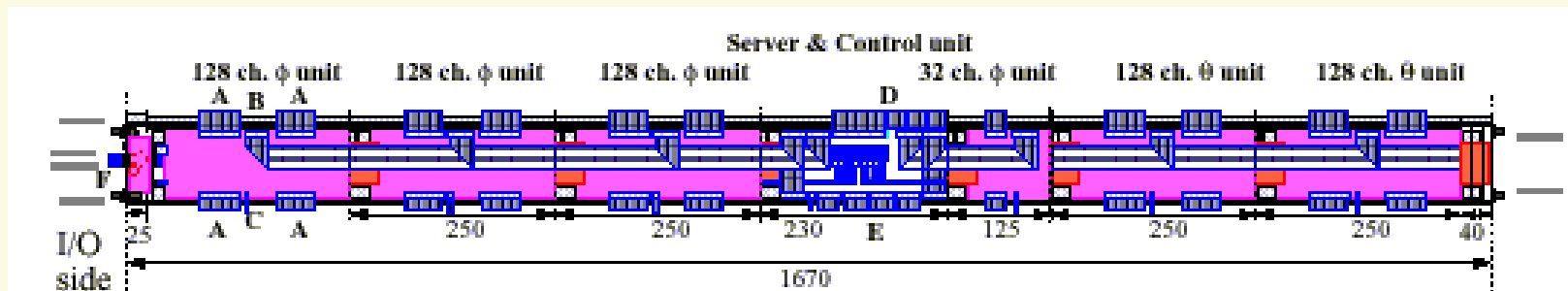
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DT Chamber Electronics layout



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DT Chamber Trigger layout



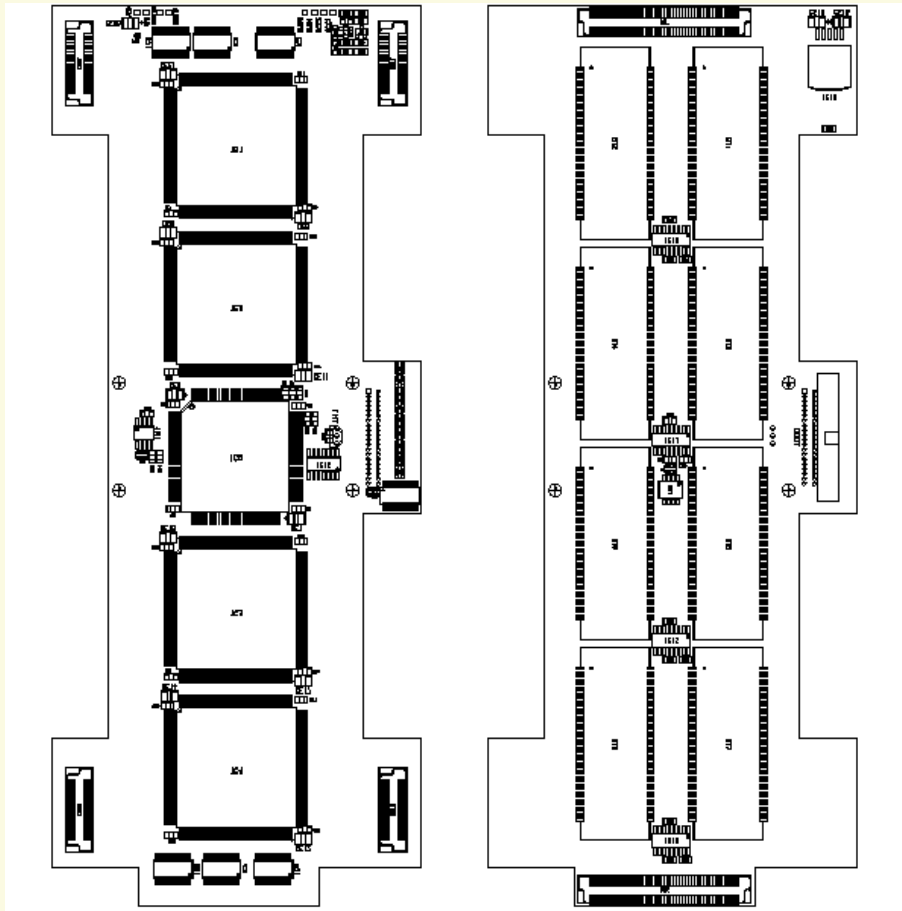
From the I/O side:

- I/O board: power decoupling, SC connectors, ...
- three 128 channels Phi_TRB: BTI, TRACO and TSS
- Server and Control board: chamber services, SC interface
- one 32 channels Phi_TRB: BTI, TRACO and TSS
- two 128 channels Theta_TRB: BTI

Each PCB has connections to its neighbours for control signals distribution. Chamber signals are received via flat cables connecting the ROB to the FE boards (A). Each TRB sends trigger data to the Server board using a dedicated flat cable (B). Each ROB is connected to the Sector Collector via a dedicated serial link (C). The Server and Control unit has connections to chamber electronics (D) for monitoring and control purposes, and connections to the Sector Collector for trigger data transmission (E).

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DT Chamber PHI Trigger board



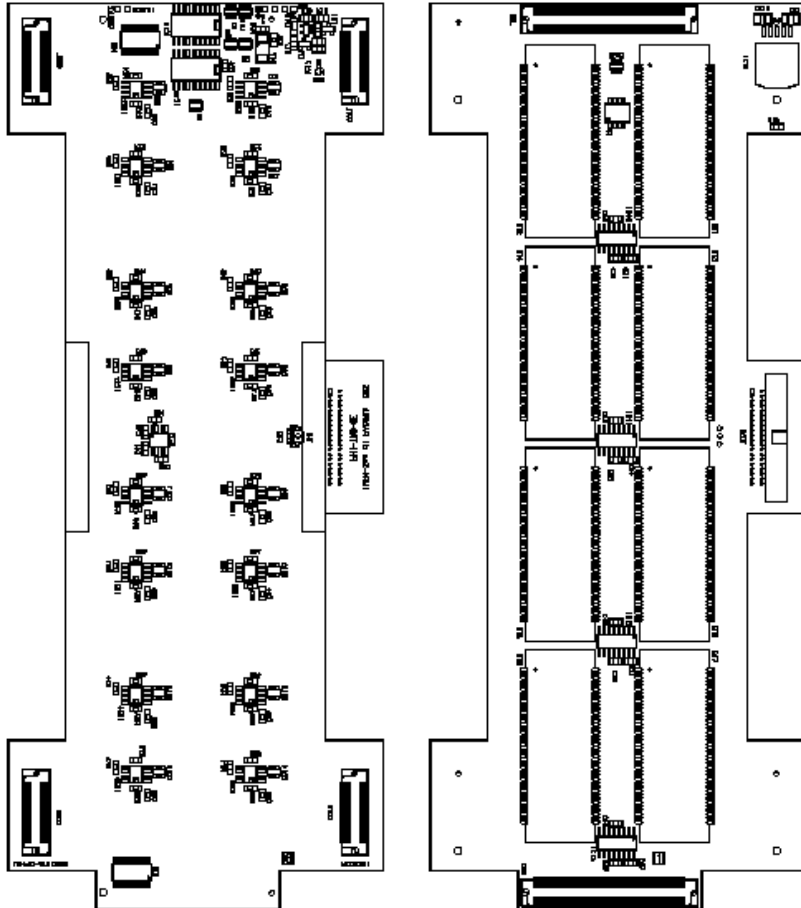
PHI_TRB

- 128 trigger channels
- 3.3V 10W power supply
- 40MHz clock

- > 8 BTIM + 4 TRACO + 1 TSS
- > single PECL clock input @ 40MHz
- > low skew clock distribution
- > temperature sensor
- > JTAG circuitry
- > low-drop regulator with over-voltage and over-current protection
- > on/off control and isolation switches

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DT Chamber THETA Trigger board



THETA_TRB

- 128 trigger channels
- 3.3V 10W power supply
- 40MHz clock

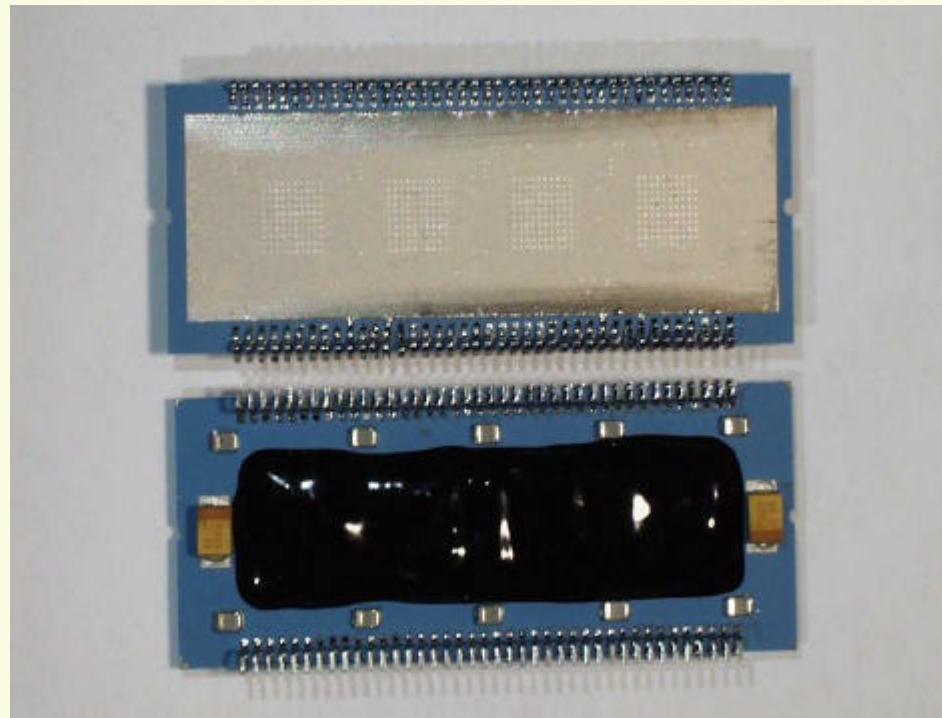
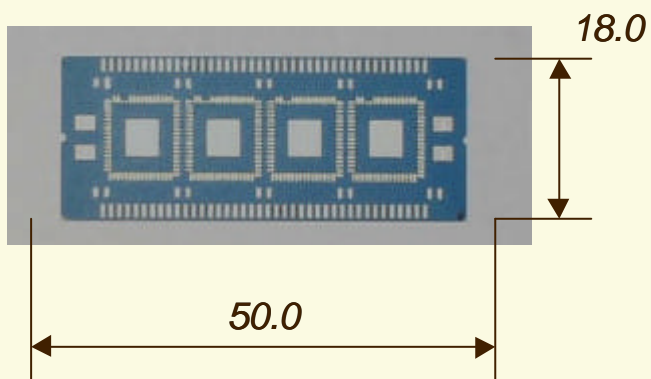
- > 8 BTIM
- > single PECL clock input @ 40MHz
- > low skew clock distribution
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- > on/off control and isolation switches

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BTI Multi-Chip Module

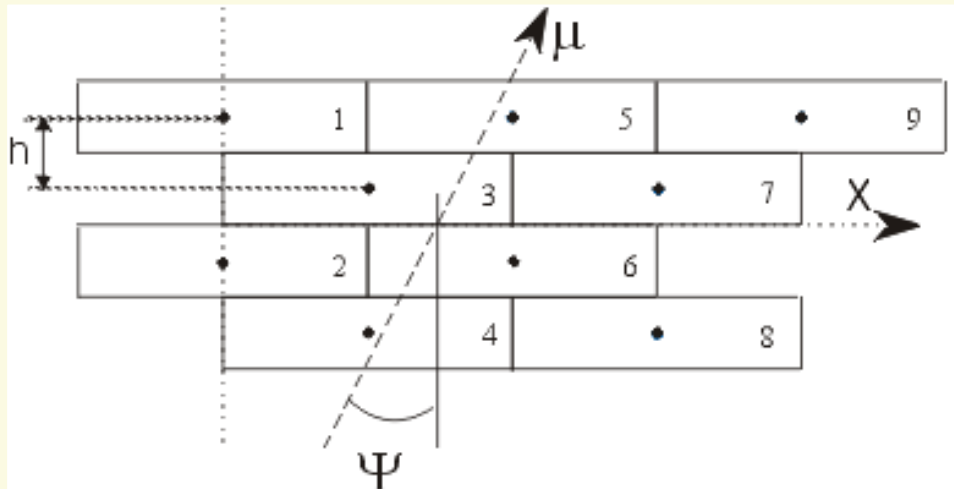
LTCC substrate

- 4 BTI dies
- 3.3V 0.85W
- 80 I/O
- 40MHz and 80MHz clocks



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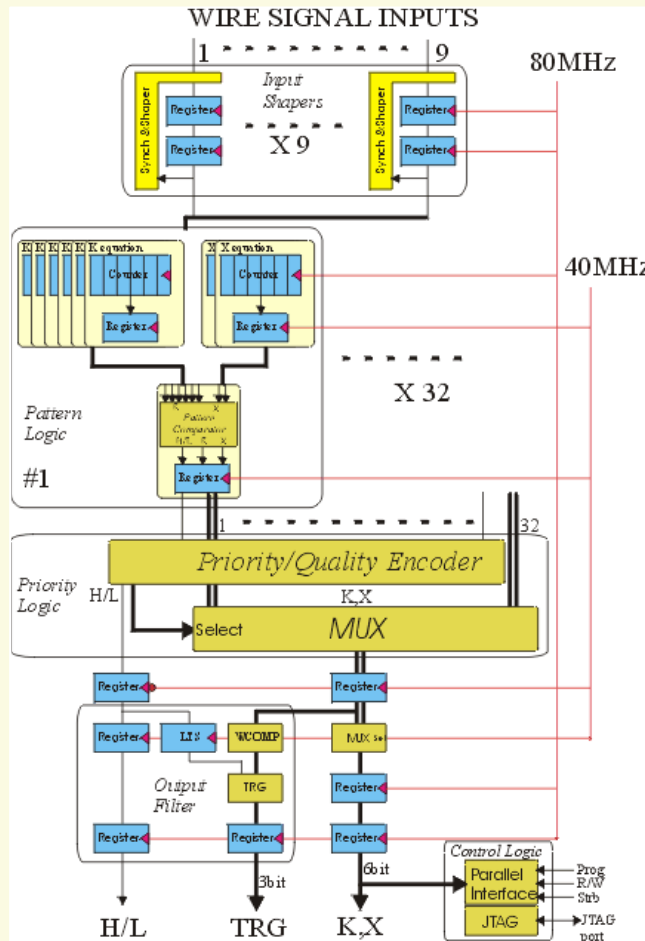
BTI Functionality



- Detection of single tracks on 9 wires
- Trigger on 3 and 4 out of 4 hit planes with quality flag output
- Track angle and position calculation
- Input signal edge triggered with programmable dead time
- Programmable drift velocity parameter
- Programmable angular acceptance
- Programmable low quality trigger suppression (LTS)
- BIST circuitry and JTAG interface
- Programming via JTAG and Parallel Interface
- 3.3V 250mW, 80MHz sampling clock
- 0.5 μ m CMOS (ATMEL) with 67k gates and 64 I/O.

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BTI Block Scheme



Input signals sampling and shaping at 80MHz

Track pattern detection and impact parameters calculation

Pattern selection

Angular filter and LTS logic

Control logic

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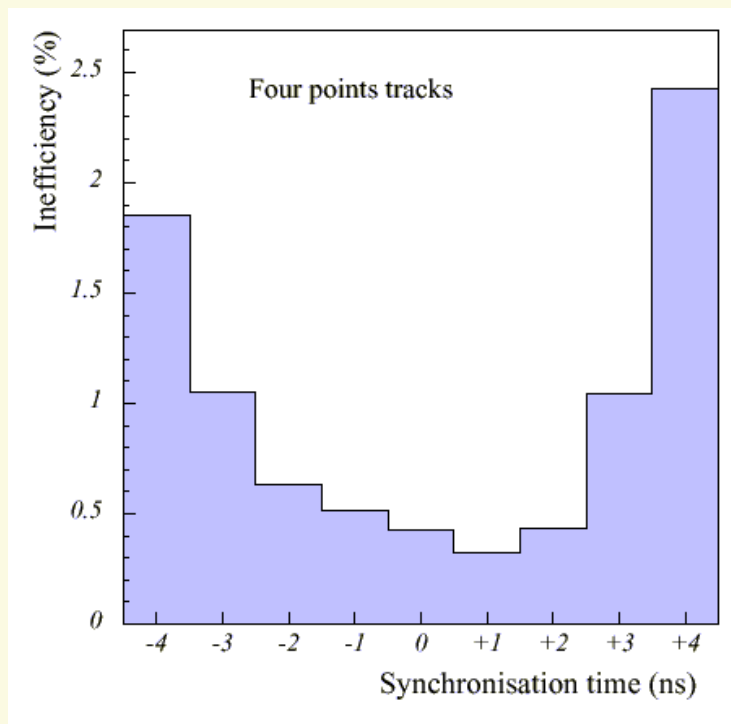
BTI: Documents

- ✓ Overview and performances of chamber trigger:
 - “Design and Simulations of the Trigger Electronics for the CMS Muon Barrel Chambers”, Ist Workshop on Electronics for LHC Experiments, 1995.
- ✓ FPGA prototype test:
 - “Beam Test Results of a FPGA Prototype of a Front-end Trigger Device for CMS Muon Barrel Chambers”, IInd Workshop on Electronics for LHC Experiments, 1996.
 - “Efficiency studies of the front-end trigger device of the muon drift tubes for the CMS detector at LHC”, NIM A 398, 1997.
- ✓ Full performance prototype test:
 - “Local Track Reconstruction for the First Level Trigger in the CMS Muon Barrel Chambers”, IVth Workshop on Electronics for LHC Experiments, 1998.
 - “Test results of the ASIC front-end trigger prototypes for the muon barrel detector of CMS at LHC”, NIM A 438, 1999.
 - “Current knowledge of BTI performance in magnetic field”, CMS Note 2000/044.

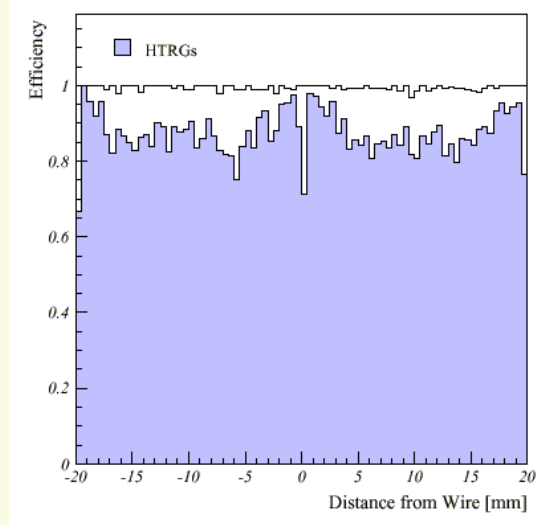
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BTI Performance: efficiency

Efficiency at normal incidence for different synchronization acceptance windows



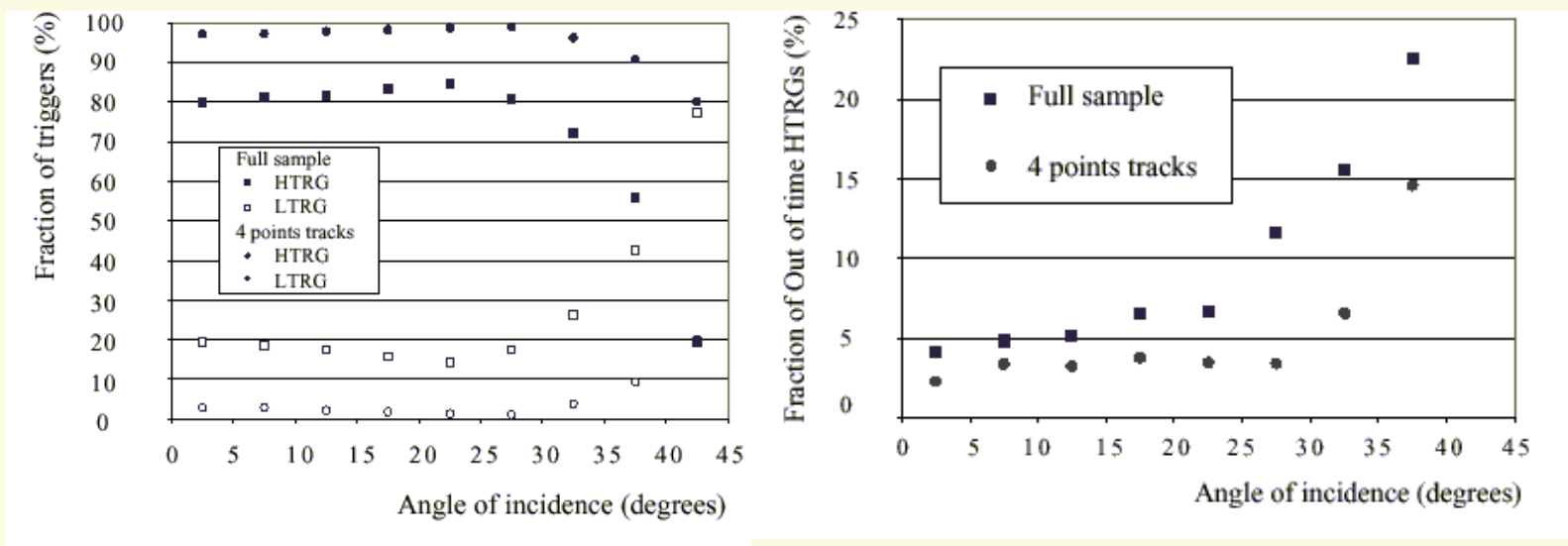
Synchronization range	$\pm 2\text{ns}$	$\pm 4\text{ns}$	$\pm 6\text{ns}$	$\pm 8\text{ns}$	$\pm 10\text{ns}$	$\pm 12\text{ns}$
HTRG fraction	84.3%	83.0%	81.7%	79.0%	75.0%	70.5%
LTRG fraction	14.5%	15.4%	16.7%	19.4%	23.3%	27.8%
Efficiency	98.8%	98.5%	98.5%	98.5%	98.3%	98.3%



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BTI Performance: efficiency

Efficiency and noise versus track incidence angle



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BTI Performance: efficiency

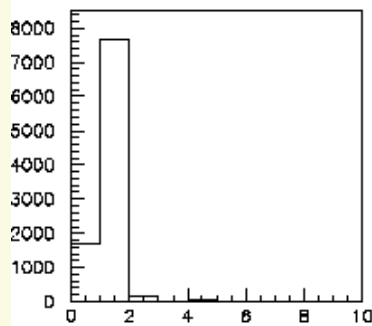
Efficiency for different configurations

BTI acceptance	LTS	HTRG fraction	LTRG fraction	Inefficiency
Standard	off	84.0%	15.6%	0.3%
Standard	on	85.1%	13.6%	1.3%
Minimum	on	70.7%	28.2%	1.1%
Maximum	on	84.8%	13.8%	1.4%

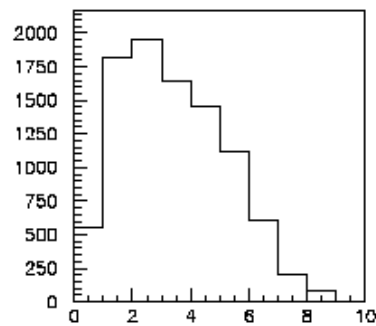
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BTI Performance: bx identification

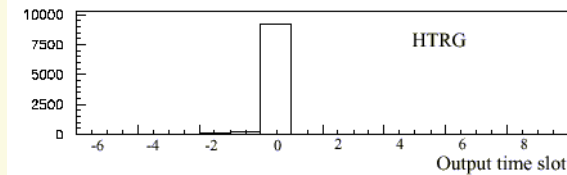
BX Efficiency and noise



Number of HTRGs per event

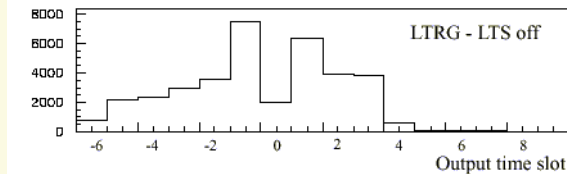


Number of LTRGs per event



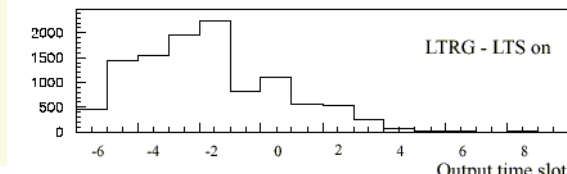
HTRG

Output time slot



LTRG - LTS off

Output time slot



LTRG - LTS on

Output time slot

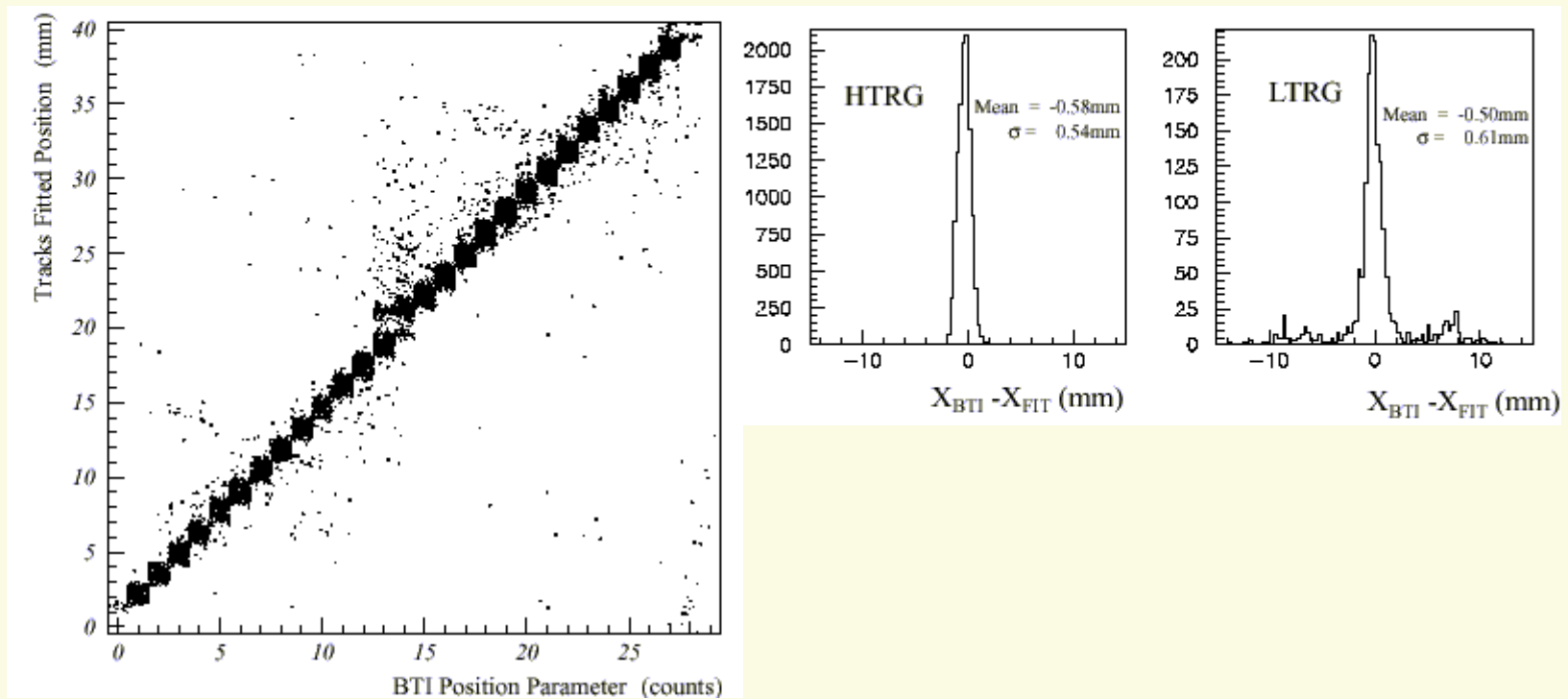
BTI acceptance	LTS	%H out of time	%L out of time
Standard	off	3.0%	351.2%
Standard	on	3.1%	148.2%
Minimum	on	1.1%	175.6%
Maximum	on	4.1%	165.3%

Table 4 – Average fraction of out of time triggers

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BTI Performance: position measurement

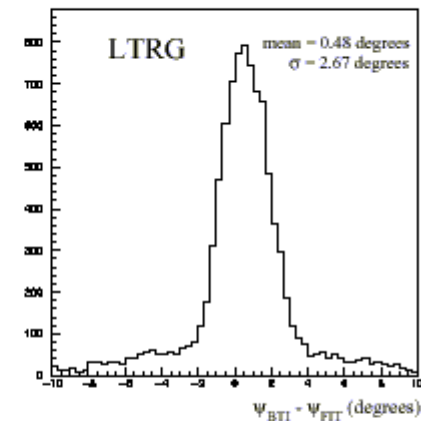
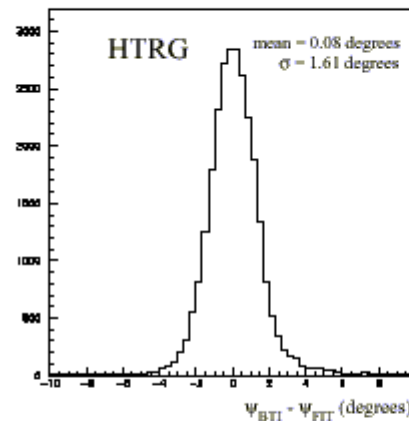
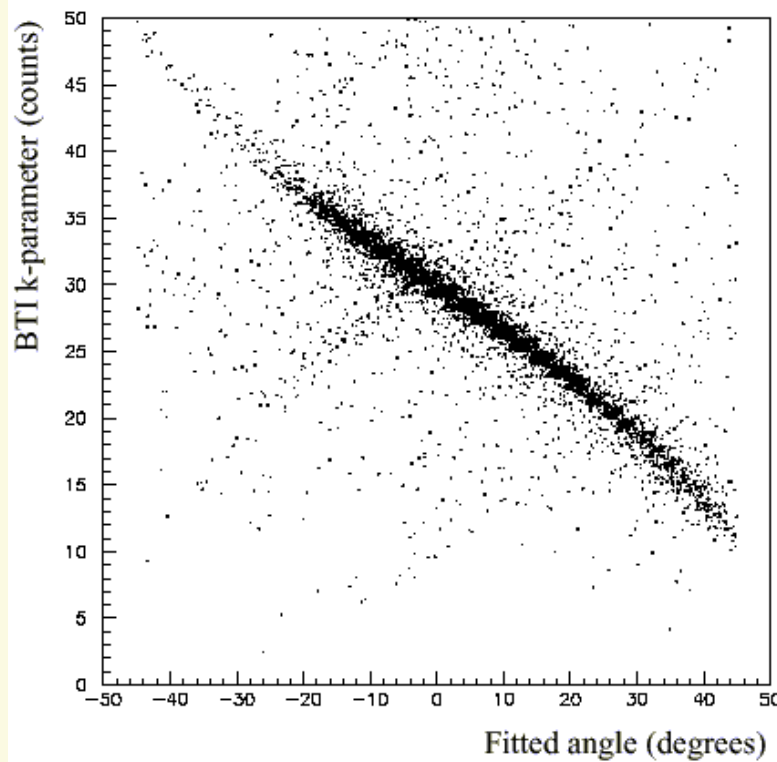
Accuracy of track position measurement



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BTI Performance: angle measurement

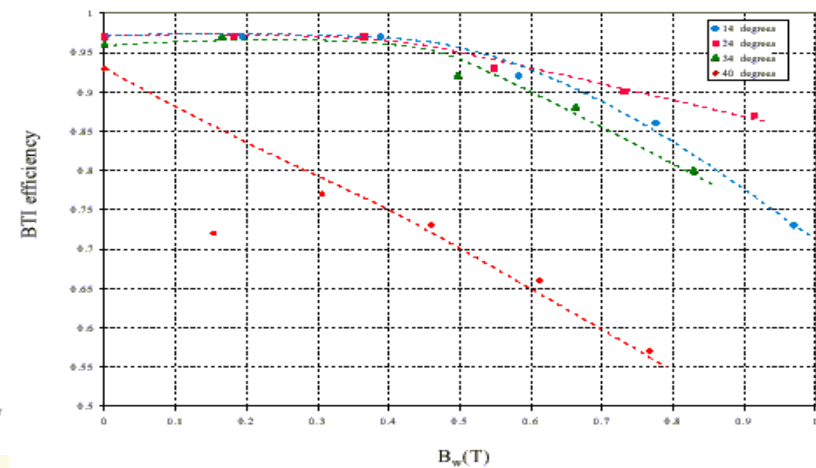
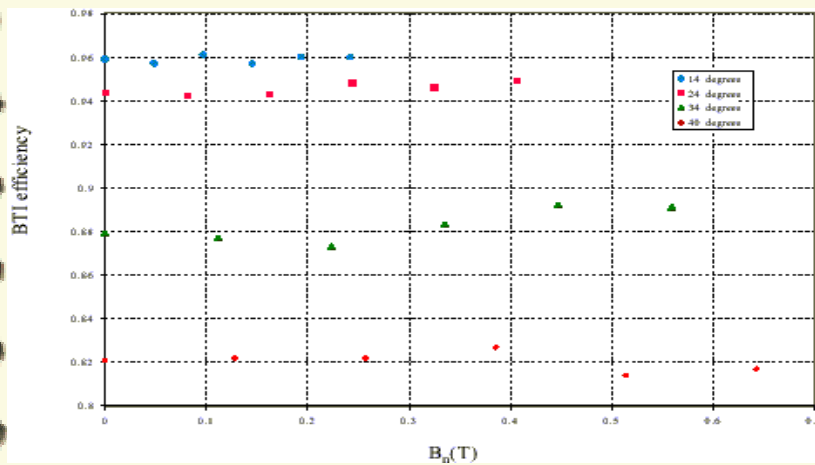
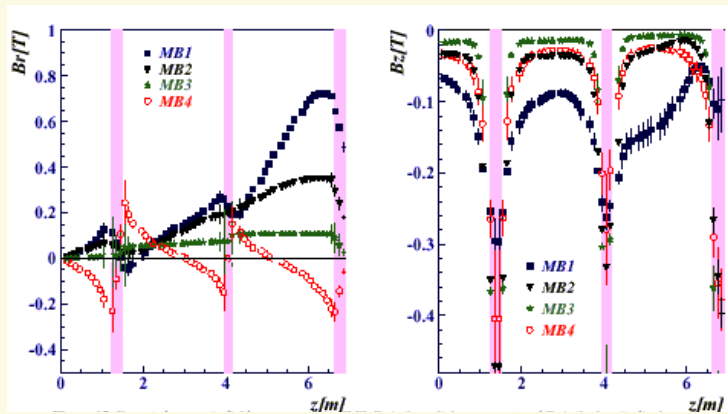
Accuracy of track angle measurement



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BTI Performance: magnetic field

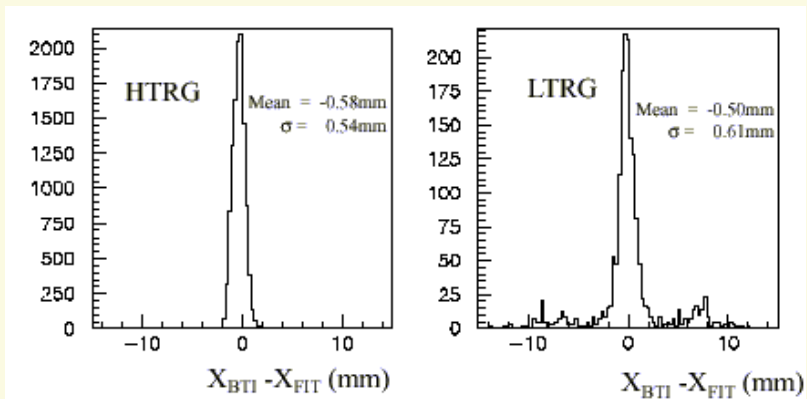
Magnetic field effects



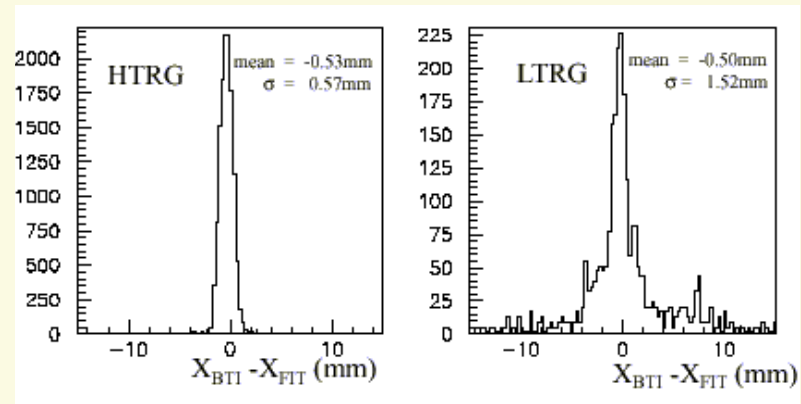
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BTI Performance: gamma rays background

Gamma rays background affects track position accuracy



Gamma rate = 10Hz/cm²



With gamma rays background

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BTI Performance: gamma rays background

Gamma rays background affects efficiency

Gamma rate = 10Hz/cm²

	%HTRG	%LTRG	Inefficiency	%H out of time	%L out of time
No Radiation	84.0%	15.6%	0.3%	3.0%	351.2%
Radiation 10 Hz/cm ²	83.0%	16.6%	0.5%	2.5%	800.0%

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BTI Performance: neutron tolerance

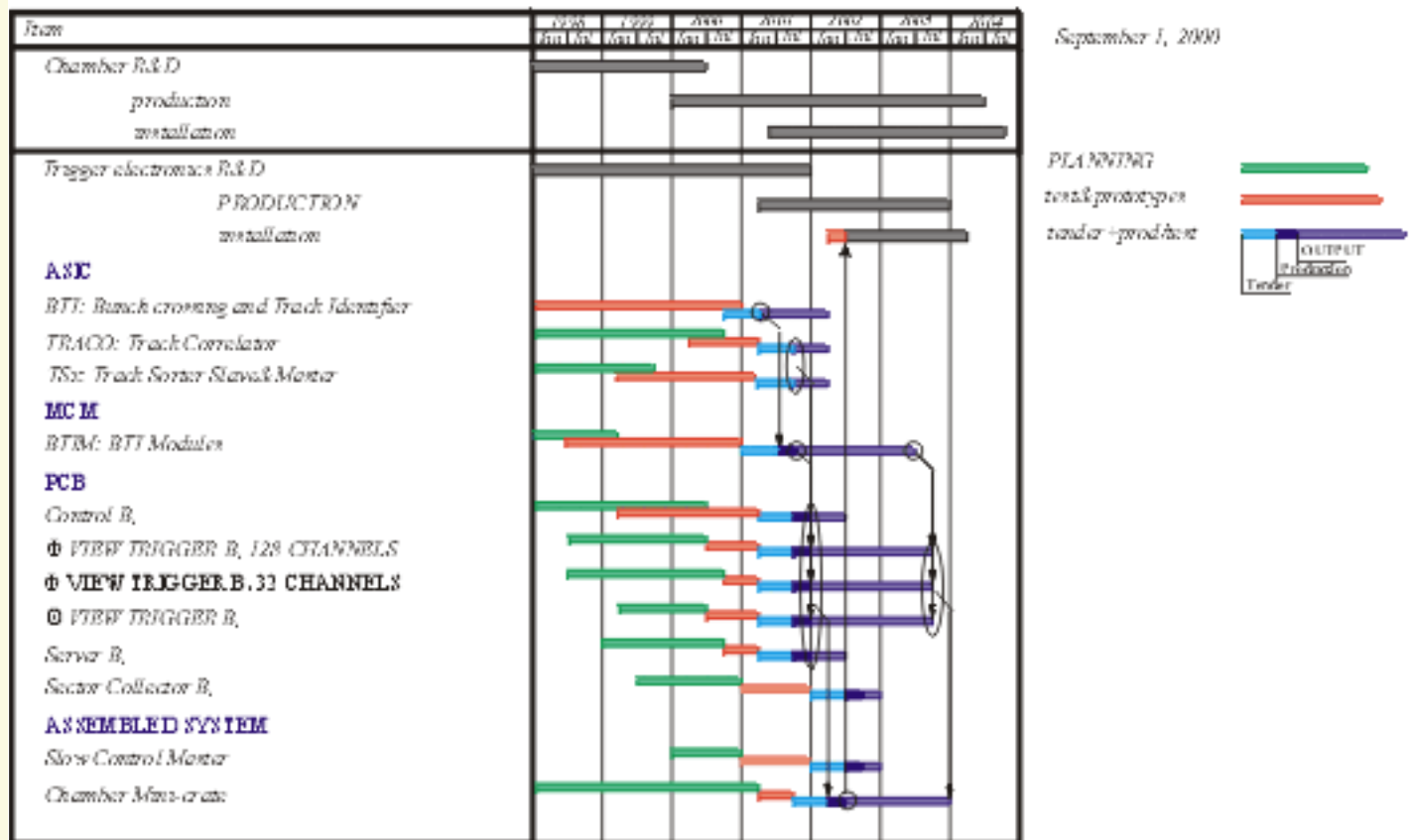
Neutron tolerance

Device	SEU cross section (cm ²)			Mean Time Between Failures (hours)		
	Thermal	LNL	UCL	Thermal	LNL	UCL
LD reg	< 1.38x10 ⁻¹⁶	< 1.40x10 ⁻¹⁶	< 1.00x10 ⁻¹⁶	< 64	< 15587	< 147892
μP	< 1.38x10 ⁻¹⁶	< 1.40x10 ⁻¹⁶	3.85x10 ⁻¹⁶	< 385	< 95340	23088
FLASH	< 1.38x10 ⁻¹⁶	< 1.46x10 ⁻¹⁶	< 1.00x10 ⁻¹⁶	< 385	< 91101	< 474734
SRAM	(1.13±0.2)x10 ⁻¹⁶	(7.03±0.2)x10 ⁻¹⁶	(1.03±0.2)x10 ⁻¹⁶	23.5	1263	23
EPROM	< 1.38x10 ⁻¹⁶	< 1.61x10 ⁻¹⁶	< 1.00x10 ⁻¹⁶	< 385	< 83043	< 474734
Optolink	< 1.38x10 ⁻¹⁶	< 1.43x10 ⁻¹⁶	< 1.00x10 ⁻¹⁶	< 385	< 93231	< 474734
ASIC TSS	< 2.68x10 ⁻¹⁶	< 9.46x10 ⁻¹⁶		< 33	< 32225	
ASIC BTI	< 1.75x10 ⁻¹⁶	< 1.31x10 ⁻¹⁶	< 1.00x10 ⁻¹⁶	< 1.5	< 507	< 4436

No measurable degradation was observed after 10¹² n/cm².
No SEE were observed.

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Project Schedule



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BTI: Project Status

- ✓ BTI and DT chamber prototypes tested:
 - with muon beams and cosmic rays
 - with muon beams and radiation background (GIF)
 - with muon beams in high magnetic fields
- ✓ BTI tests in radiation background:
 - 10krad in gamma cell (2krad/minute)
 - thermal neutrons up to 10^{10} n/cm²
 - fast neutrons from reactor (Prospero) up to 10^{11} n/cm²
 - fast neutrons (< 10MeV) from d-Be reaction up to 2×10^{12} n/cm²
 - fast neutrons (< 60MeV) from p-Be reaction up to 10^{12} n/cm²

Functional behaviour and performance are fully satisfactory.

After irradiation tests up to the reported levels no degradation in the electrical or functional characteristics was measured. No SEE was observed.

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BTI: Project status and future developments

✓ *Status and known problems:*

- The ATMEL foundry in Europe has been closed. Only 1400 dies are still available from the first prototyping batch. The next batch could be produced by ATMEL in USA after a new prototyping phase and with 30 weeks of mask processing time.
- BTIM prototypes with LTCC substrate have low yield, about 40%.

✓ *Future developments:*

- The BTI/BTIM tender must start as soon as possible to account for the unexpected delay needed by ATMEL to start chip production. A new prototyping batch could be received within mid 2001 placing the order for BTI production in December 1999.
- In order to gain time for BTIM production the tender must be anticipated and the 1400 available dies must be used for further prototyping.
- BTIM production schedule:
 - 50 pcs by September 2001
 - 950 pcs by December 2001
 - 5 lots of 2300 pcs from March 2002 to June 2003.

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