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Sector Collector LVDS receiver board

User Manual – V 1.0

Introduction

It is a 6U VME board realizing the Sector Collector LVDS receiver section, for trigger signals coming from two chambers. Board I/O is continuous and syncronous with a clock (40 MHz), with no local data storage. Therefore, the board must be used together with storage devices, like Pattern Units. At each clock the board input consists of 160 bits. Also the output consists of 160 bits, plus 8 *lock* bits which represent the lock status of LVDS receivers.
Input is fed via 4 Ethernet cables (Cat. 6, 4x2 pairs), having 60 m maximum length and connectorized with RJ45 plugs, crimped according to *568B Standard.*
Output is fed through 8 flat cables (68 pin, pitch 0.635 mm), connectorized with Pattern Unit like connectors (Cern SCEM 09.55.21.068.9).

Power

The board needs 2 power levels, 5 V and 3.3 V, which can be provided either externally, through a 4 pin AMP connector, or via VME and on-board power regulators. The different power modalities are selectable via jumpers, as reported in the following table.

5 V power source	3.3V power source	Comment	Jumper settings		
			JP1	JP2	JP4
5 V VME	Regulated 5 V VME	Recommended	open	1-2	1-2
Regulated 12 V VME	Regulated 5 V VME	Big dissipation	1-2	1-2	2-3
5 V external	Regulated 5 V external	Recommended	open	2-3	1-2
Regulated 12 V external	Regulated 5 V external	Big dissipation	2-3	2-3	2-3

Reference Clock

A 40 MHz reference clock can be provided either externally via LEMO 00, or using a local 40 MHz oscillator. This clock is not needed to be in phase with data clock. The clock source is selectable through the jumper JP3: position 1-2 is for external clock, 2-3 for internal clock.

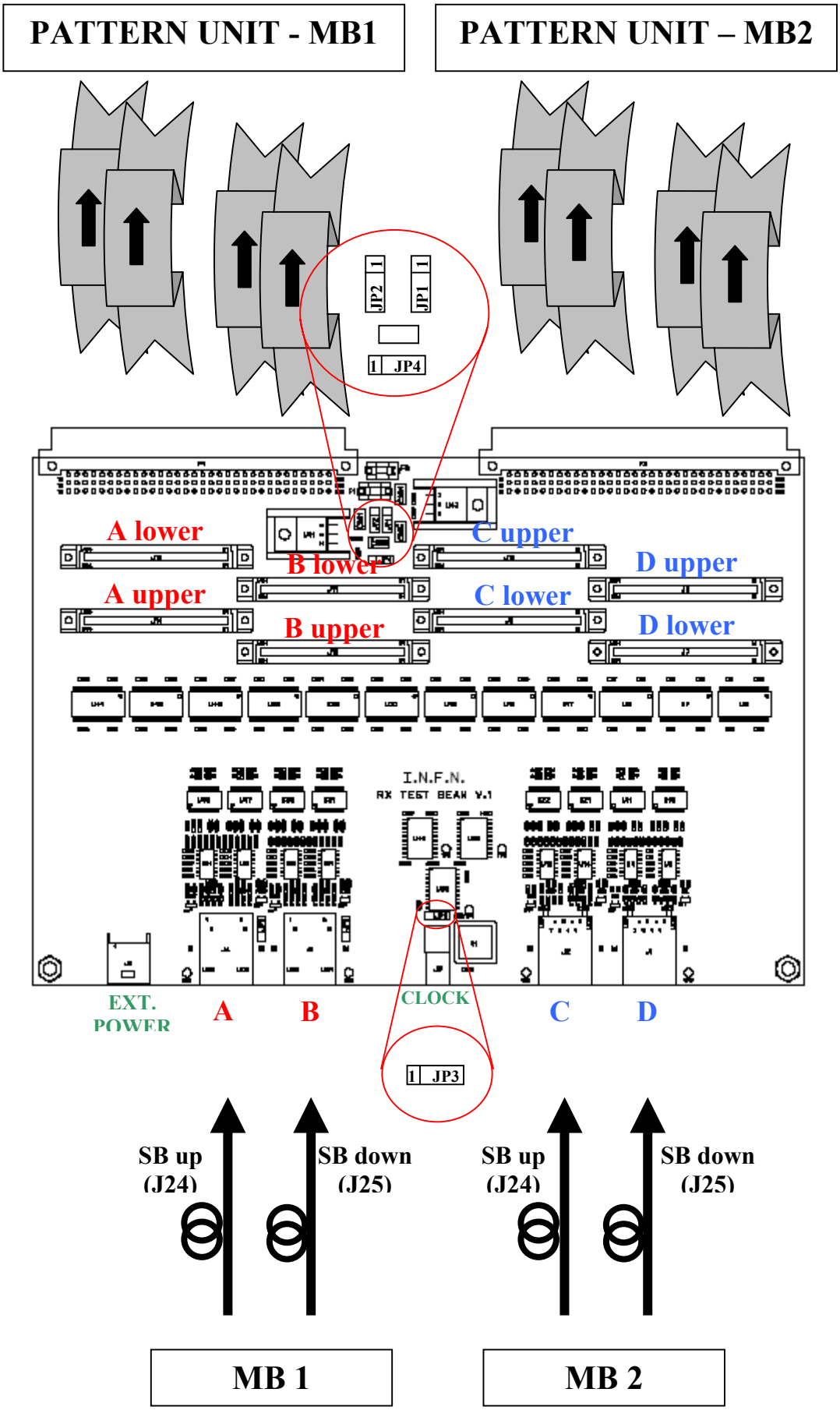
Operating notes

To check if LVDS receivers are properly working, i.e. into a *locked* state, watch the two LEDs placed on the front of each RJ45 socket: they should be lighted.
In order to obtain such a condition check that:

- ethernet RJ45 plugs are connected on both ends;
- LVDS trasmitters (Server Boards in minicrates) are on;
- the LVDS receiver board is on and clocked.

However it could happen the LEDs stay off. In this case, power cycle the receiver board while the reference clock is off, then supply the reference clock signal. LEDs should now turn on.

Example setup for MB1 and MB2 chambers



I/O Data Format

SB to SC – Ethernet cables A (MB1) &C (MB2) – SC Input						SC Output	
RJ45 pin	**Input signal name (SB side)**	**Bit**	**Info**	**Notes**	**Null value**	**Flat cable A & C**	**Bit**
1+ 2-	TRK12_UP	0-9	ϕr = 0-11	11 = sign bit, comp. 1	0	Lower	0-9
				LVDS Lock (0=locked)		Lower	10
3+ 6-	TRK12_UP	10-19	ϕb = 12-21	21 = sign bit, comp. 1	0	Lower	16-25
				LVDS Lock (0=locked)		Lower	26
4+ 5-	TRK12_UP	20-25	Qual = 22-24 I/II trk = 25	Encoded & Inverted 0=1st; 1=2nd	0	Upper	0-5
	BCRESET_UP	26	BC0	From TTC, -ve logic	1	Upper	6
	PARITY_UP	27	Parity	Bit 0-25; 0/1=even/odd	0	Upper	7
	CAL_UP	28	Calibration	From CCB, -ve logic	0	Upper	8
	CCB_RDY_UP	29	CCB ok	+ve logic	1	Upper	9
				LVDS Lock (0=locked)		Upper	10
7+ 8-	TRG_θ	30-37	Theta = 0-7	DT wire mapping ?	?	Upper	16-23
	BCNT_θ0	38	BX# bit0	From TTC	---	Upper	24
	BCNT_θ1	39	BX# bit1	From TTC	---	Upper	25
				LVDS Lock (0=locked)		Upper	26

SB to SC – Ethernet cables B (MB1) &D (MB2) – SC Input						SC Output	
RJ45 pin	**Input signal name (SB side)**	**Bit**	**Info**	**Notes**	**Null value**	**Flat cable B & D**	**Bit**
1+ 2-	TRK12_DW	0-9	ϕr = 0-11	11 = sign bit, comp. 1	0	Lower	0-9
				LVDS Lock (0=locked)		Lower	10
3+ 6-	TRK12_DW	10-19	ϕb = 12-21	21 = sign bit, comp. 1	0	Lower	16-25
				LVDS Lock (0=locked)		Lower	26
4+ 5-	TRK12_DW	20-25	Qual = 22-24 I/II trk = 25	Encoded & Inverted 0=1st 1=2nd	0	Upper	0-5
	BCRESET_DW	26	BC0	From TTC, -ve logic	1	Upper	6
	PARITY_DW	27	Parity	Bit 0-25; 0/1=even/odd	0	Upper	7
	CAL_DW	28	Calibration	From CCB, -ve logic	0	Upper	8
	CCB_RDY_DW	29	CCB ok	+ve logic	1	Upper	9
				LVDS Lock (0=locked)		Upper	10
7+ 8-	HL_θ	30-37	Theta = 0-7	DT wire map? values?	?	Upper	16-23
	BCRESET_θ	38	BC0	From TTC, -ve logic	?	Upper	24
	TRGOUT_θ	39	Trigger	From CCB, logic?	?	Upper	25
				LVDS Lock (0=locked)		Upper	26