Appendix

A review of the electronics residing on board of Barrel Muon Chambers has been made together with the CMS Electronics System Coordinator G.Stefanini on the 18 December 1998.
The results are reported in the attached document **(a).**

Neutron tests on electronics boards have been performed at Prospero facility in Valduc (F) on the 27 and 28 April 1999. Six high voltage distribution boards (HVB), three front end boards (FEB), one control board (CCB), two sets of LVDS chips and a set of glue joints were tested at different neutron fluence as in the attached layout **(b).**
The final results of the High Voltage tests on the irradiated boards are in **(f)** .
An outgassing test has been performed after the electrical tests on a board irradiated at ~2*10exp12 N/cm^2 ; results in http://warco.pd.infn.it/cms/electronics/prospero-outgas.ps

Preliminary results on FEB's are in **(c)**. The final results of the checks on the FEB's are located at: http://wwweda.pd.infn.it/cms/DTFB/electronics/frontend/documenti/radiation.pdf

Concerning the FR-4 outgassing, statements by Mr Tavlet - TIS quoted in the review report, indicate that any outgassing under irradiationin Barrel MU conditions is negligeable; nevertheless outgassing tests under irradiation have been performed on FR-4 printed circuit boards and resuls are located at:
http://wwwae.ciemat.es/~willmott/fr4_outgassing_tests.ps

An aging test performed to check for negative effects on the efficiency, due to all materials included in the chamber, indicates that HV boards and FEB's do not have any effect for an integrated charge on the wires equivalent to at least 10 LHC years life.

Concerning the use of FR-4 PCB's with respect to safety prescriptions by CERN, we stress the fact that, at the present stage of the CMS Barrel Muon project, there is no practical chance to find a viable substitute to this material for electronic PCB's.
So we will go on with the present materials in accordance to the "Interim Action Plan", in particular point 1., stated in the attached Memorandum by the Technical Coordinator and GLIMOS about the "Possible replacement of FR-4 laminates and printed circuit boards" **(e).**

(a)

Report on the mini-review of CMS Muon DT front-end electronics embedded in the chamber

PART A

Internal (and informal) review - CERN 18 December 1998

Participants: M. De Giorgi, M. Pegoraro INFN Padova
A. Marchioro, G. Stefanini (chairing) CERN

1 . Motivation and objectives

The review has been requested by the muon project manager following the recent EDR. The muons intend to start production of the chambers early in 1999. A part of the front-end (FE) electronics is embedded on the chamber, and its production is therefore constrained to start at the same time as the chambers themselves. A full electronics review will take place in 1999, at a date that is not yet fixed, but certainly too late to fit in the chamber production plan. It has therefore been agreed to carry out a partial review of the proposed embedded electronics, to assess its production readiness and to verify that it does not contain any unacceptable high risk features, particularly with respect to radiation tolerance.

2 . FE electronics overview

The embedded FE electronics that is the subject of this review consists of a 16-channels front-end board (FEB), and an HV distribution board (each chamber).

Each FEB contains 4 identical readout (BiCMOS) custom ASICs and 1 interface commercial (CMOS) IC. The ASIC has been designed by M. Pegoraro.

The PCBs currently used are made in the standard FR4 material.

The internal grounds make use of copper strips spot-welded to the chamber aluminium plates. The electrical ground is connected to the chamber body.

The embedded electronics interfaces with the mini-crate electronics, which is mounted on the outside of the chamber, and is not part of this review.

3 . Review of the FE ASIC

3.1 General

The ASIC is a full-custom design in 0.8um BiCMOS AMS technology. It uses about 500 transistors/chip. mostly bipolar. A chip contains 4 readout channels. Each channel contains a charge amplifier, baseline restorer and comparator (with external reference and threshold voltages). The output pulse is stretched and sent to the LVDS output driver. The ASIC also includes a temperature sensor. The nominal power consumption is 25mW/ch, or 400mW per FE board. The LV power supplies are +5V (analogue) and +2.5V (LVDS drivers). The chip is currently packaged in a 28 pin ceramic leadless chip carrier (CLCC).

The reference and threshold voltages, common to all channels in a chip, are generated and provided by the mini-crate electronics located outside the chamber. These levels are bussed over lengths up to about 1m. The requirements on threshold voltage accuracy and noise can be appreciated by considering that 9mV correspond to a 3fC threshold. The typical spread of 0.13fC implies that the noise on the line must be smaller than 0.5mV rms.

3.2 Experience with ASIC chips and FE boards

The ASICs from one MPW run have been fully characterized in the lab in 1998. Of the 100 untested samples delivered, 86 passed the functional and acceptance tests.

A system of 18 FE boards (ie about 200 channels) has been tested on chambers at CERN in GIF. The measured performance appears to meet the requirements. The main results were outlined by M. Pegoraro in this review, and have been published.

3.3 Plans for ASIC production

The new submission was done on 8 Dec 98 and the delivery of the chip is scheduled in early March 99. The purchase order could be submitted to the foundry (AMS) in June 99. Negotiations are under way on the possible wafer probe testing by the vendor.

4. Points of concern and recommendations by the reviewers

4.1 FE ASIC

No evidence of weak points in the design was found. Some concern was expressed on the following points:
a) stability and noise of the reference and threshold voltages that the chip receives from the mini-crate outside the chamber. The best practices of shielding and filtering should be used;

b)the chip will eventually be delivered in a QFP44 package, with longer internal bonding contacts. Impact on crosstalk needs to be assessed;

c) the chip has not been tested under neutron irradiation. The bipolar transistors are biased at low current (<10uA), and possible radiation damage effects cannot be excluded. These measurements need to be done as soon as possible.

Moreover, the reviewers felt that the estimated cost per wafer, reported as being quoted by the foundry, was unusually high. This point might need some clarification.

4.2 Ancillary chips
In the final layout the FE board will contain, in addition to the custom ASIC, one I2C commercial grade interface chip. This chip is available from only one source and its sensitivity to radiation, particularly single-event effects (SEE), is not known. The chip is available only in packaged form, so that SEE testing is unpractical.

The feasibility of other solutions for the I2C interface have been briefly discussed, but no definite plans have been made.

4.3 Passive components

PolySwitch resettable fuses are used for protection in the FEB. These devices are based on conductive polymers. They should be tested for possible neutron radiation damage.

It was suggested to check the FR4 PCB material under neutron irradiation for outgassing of bromine which might affect the chamber performance.

Some questions were asked on the technique envisaged for internal grounding (Al to Cu) and on the grounding configuration that will be implemented in the final system to avoid ground loops etc. Some of these points may need clarification.

The HV board contains ceramic capacitors and resistors on hybrids. It was suggested, for safety, to test the board under neutron irradiation.

5 . Reviewers' conclusion

There is no evidence of flaws or excessive risks that prevent starting the production of the ASIC and board according to the proposed muon planning. However several points of concern need were raised and need clarification by tests that could be carried out during the pre-production phase in the first half on 1999.

This draft report was sent to the Padova team on 15 January 1999.

PART B

Comments received from INFN Padova and CERN –TIS

On point 4.1

When moving from the present package to the final one (QFP44), the length of the bonding wires in the ASIC package (currently about 3mm) will increase by 1mm at most. This is not likely to cause any significant problems.

The ASIC transistors biased at low current are used in a reference source and in a thermal sensor. Should any degradation be observed following neutron irradiation (to be carried out soon), a modification to these transistor stages is possible and straightforward.

On point 4.3, as from discussions with M. Tavlet/TIS

In the muon chamber, the radiation dose (including neutrons) will be much too low to induce any damage in polymeric materials.

The radiation dose will also be too low to induce significant outgassing from plastics.

The use of FR-4 is in principle forbidden at CERN because of the bromine content (IS-41). CERN/TIS is consulting vendors in view of finding alternative suitable materials.

PART C

Final remarks and recommendations from reviewers

From various discussions it is understood that the DT muon team will measure the resistance under neutron irradiation of the various elements (ASICS, boards, HV cables). This is now scheduled in the last week of April 1999, at the PROSPERO reactor facility near Dijon;

The question on the PCB material (FR-4) had been raised by the reviewers mainly in view of the potential, even minimal, outgassing of bromine compounds into the chamber gas. This may well be a totally negligible risk and the muon team is best placed to assess it.

However, the FR-4 issue is currently receiving much attention the general case of PCB for electronics modules, because of environmental considerations (release of bromine compounds in case of fire). As already pointed out, the use of FR-4 is generally tolerated but is in fact in violation to CERN safety rules (IS-41). However a suitable material of improved compliance is not yet available. This point was on the agenda of the CMS Technical Coordination Meeting of Monday 8th February, where R. Schmidt reviewed the issue and made some recommendations for an interim CMS strategy (see the minutes for further details). In any case switching from well proven (performance-wise) materials to new ones may imply high risks and can only be envisaged after a thorough technical evaluation.

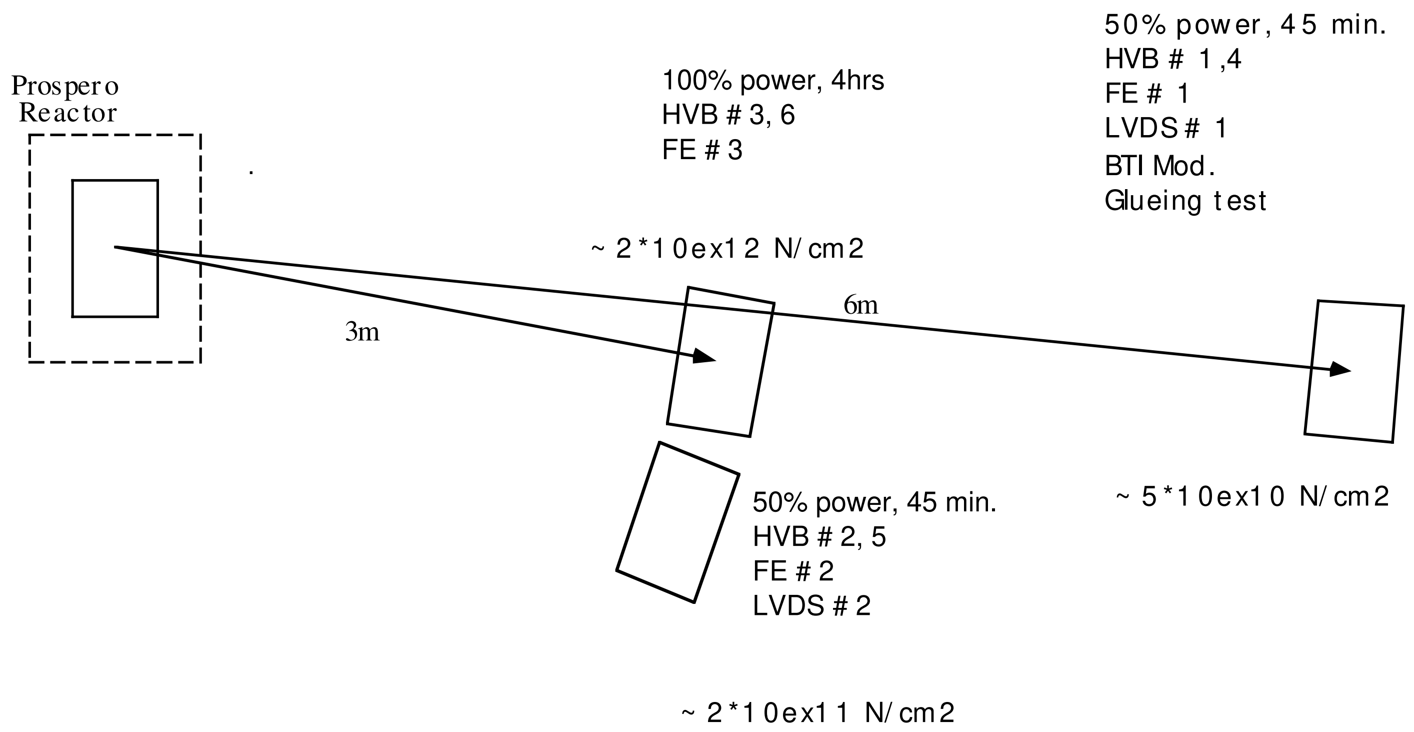
In the present case, the reviewers think that there is no realistic alternative, within the project deadlines, to the use of standard PCB material.

In conclusion, the reviewers confirm that to the best of their judgement there is no evidence of excessive risks that prevent starting the production of the ASIC and board according to the proposed muon planning, once the tests mentioned above have given satisfactory results.

A. Marchioro, G. Stefanini 1 March 1999

(b)

Prospero -Test Layout



PROSPERO TESTS

3 frontend boards have been exposed at Prospero facility to a total neutron flux of 5x10**10, 2x10**11 and 2x10**12 respectively; for the first two boards that have been already tested after exposure we have found no functionality problems even for the commercial chips (I2C interface & HCT glue logic). For what concerns performances no difference has been found between before and after irradiation tests that regarded noise, sensitivity and time response. No change has been detected in power consumption of either card.

AGEING TESTS

10 MAD prototypes have withstood a period of 2000 hours at 125 degrees centigrade ambien temperature while powered. None of the chip died and at the end of this period a test on noise and sensitivity revealed that while gain and threshold accuracy were maintained noise has increased by about 30% (it has to be noticed that the lifetime accelerating factor is about 1000). During the whole period other characteristics of the chips have been monitored and checked, including temperature sensors and behaviour at high temperature, and no major problems were detected.

RESISTANCE TO HV DISCHARGES

Extensive tests have been performed on circuits and components for protecting the frontend chip against accidental discharges of the detector high voltage. A good protection has been found, capable of withstanding a complete discharge of the 3.5 KV applied to the wire, that doesn't spoil speed and noise performances.

May, the 3rd 1999

MEMORANDUM

>From : Technical Coordinator and GLIMOS

To : all Project Leaders: to pass on to persons concerned

Subject : Halogen-free materials at CERN;
Possible replacement of FR4 laminates and Printed Circuits.

Background

Since the design of LEP, the use of halogen-free flame-retardant cables has been imposed at CERN (cf. Safety Instruction No 23 *). Since March 1995, Safety Instruction No 41 * extends the fire-behaviour requirements to any non metallic materials to be used at CERN. These materials must be flame-retardant and, in case of fire, evolve non corrosive smoke of low optical density and low toxicity. This is of particular importance for applications in underground areas with escape routes that are often complicated. It has recently been pointed out that the substrates of printed circui boards, the usual FR-4 or FR-5, are made out of epoxy resins containing between 7 and 10% o . In case of fire, these materials will produce thick corrosive and toxic smoke, constituting a real threa for components and human lives in underground areas.

The replacement of these common materials, for which much experience has accumulated, by safer ones is a world-wide concern. A European Directive under preparation proposes the banning of such materials from the year 2004 **. International consortia of major companies (including suppliers of base materials, producers of ICs and laminates, and manufacturers of electronic circuits) are currently working to demonstrate the use of halogen-free alternatives for electronic boards conforming to the usual standards. Today some companies are already proposing such 'green' materials (see list in the attachment). But so far it is not yet known if they can be considered in large-scale commercial applications, in particular as far as PCBs are concerned.

Interim action plan

The present position of TIS in this matter has recently (March 31) been published in a memorandum (see document in the attachment). Objectives for an improved compliance with IS-41 have been stated and a subgroup of the Cable & Material Working Group has been established to study the issue, explore possibilities of supply of alternative materials, propose test-programs and establish implementation schedules. In the medium-term you are requested to:

1. Continue work with previously approved plastic laminates and PCBs in subprojects where design, testing or ordering is ongoing or already completed and where retroactive changes are generally not possible for technical, budgetary and schedule reasons. Nevertheless information about type, quantity (estimate), committed or projected ordering-date, and locations (i.e. marked on
a cross-section drawing) of the material shall be passed on to the GLIMOS who will transmit to the WG (by end of May 99);

2. Similarly, Project Leaders shall inform the GLIMOS and the Technical Coordinator about all planned foams or filling-materials containing bromine. The GLIMOS and the Technical Coordinator will, with

the help of the working group, try to find alternative materials and reserve the right to cancel any ongoing orders.

3. i) Look at suitable, published alternatives as they become available (see in the attached document), for subprojects which are starting their design, prototypes and/or tests and are still uncommitted for manufacturing.
ii) Decide together with the Technical Coordinator about the use of such a new material, in order to minimise possible risks which could be associated with materials that have not yet been produced on an industrial scale.
iii) In case it appears impossible (in terms of delay, price and/or technical problems), report to the GLIMOS, who will transmit to the WG, the reasons for not being able to use one of the replacement products.

4. If no replacement material can be found, help the GLIMOS and the WG to define and to scale the potential hazard and to propose compensatory measures for fire protection.

We count on your support and collaboration to increase the safety of our experiment and to protect the environment.

* Safety Instructions No 23 and No 41 available at the TIS Secretariat, 75097,
and on the web (http://www.cern.ch/CERN/Divisions/TIS/safdoc/instr_en.html).
** see Web site: http://www.itri.co.uk/WEEE2.htm

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High Voltage Boards @ Prospero Test
M De Giorgi G. Pitacco
27-28 April 1999

27 April at 16:00**:** **Six HVB boards mounted as in Layout**
#1, 2 coating DP490 # 3,4,5,6 coating DP190

HV @ +4kV, +/- 2kV currents in **nA** :

	I_W	I_S	I_C	
	54	13	22	(HVB #1÷6)
28 April at				
08:00: All boards ON since day before;	**22**	**7**	**12**	(HVB #1÷6)
09:15 start Fase 1: Reaxctor @ 50% **10:03** Reactor off				
10:25	45	8	14	(HVB #1÷6)
11:00	14	5	6	(HVB #3,6)
11:05 start Fase 2: Reactor @ 100% **15:05** Reactor off				
15:15	31	5	6	(HVB #3,6)

END TEST

08 September in LNL at				
11:00 All boards ON since day before	**24**	**7**	**9**	(HVB #1÷6)

CONCLUSION:

No meaningful difference was detected in leakage currents of the boards before and after irradiation.

(g)

results from enrico tests after irradiation

TIS/DI/HS/jg (99-33)   31 March, 1999

M E M O R A N D U M

To: see list in fine

From: H. Taureg and H. Schönbacher

Re: Halogen in Printed Circuit Boards

We have recently become aware that glass-fibre reinforced Printed Circuit Boards contain 7 to 10% bromine which does not conform with the CERN Safety Instruction 41. This comes at a time where design and pre-production of some LHC detector units are so far advanced that replacements by a non-halogenated material is very difficult or even at this stage impossible.

We have therefore asked M. Tavlet from TIS Commission to set up a working group with the following mandate:

- to identify the size of the problem in both LHC machine and experiments,

- to propose compensatory measures in well justified cases where replacement at this stage of the LHC project is not possible,

- to search for alternative materials and propose test programmes,

- to propose a time schedule for implementation of the new materials.

In the meantime, while work will have to continue with the materials containing bromine, all efforts shall be made to replace them, wherever possible, in a medium-term plan.

The proposed composition of the working group is given below, and we count on all your efforts and support, such that their work can be concluded in the sense of increased safety and protection of the environment.

- M. Tavlet and J. Gulley / TIS (respectively chairman and secretary)
- A. Gandi /EST-SM,
- P. Farthouat, B. Lofstedt, A. Monfort / EP
- M. d'Auria /PS-PO,
- M. Devard /SL-PO,

The first status report shall be given by mid-June 1999.

Distribution:

M. Bona, J. Fivet, C. W. Nuttall, F. Szoncso, W. Weingarten / TIS
J. May / DG
C. Benvenuti / EST
K. Fernqvist, R. Rausch / SL
J. Gruber / PS
R. Schmidt / LHC
A. Fucci, B. Heck, H. F. Hoffmann, M. Letheren, / EP
Persons mentioned in the composition of the group
Electronics Coordinators for LHC experiments: P. Farthouat /ATLAS,
G. Stefanini /CMS, F. Formenti /Alice, J. Christiansen / LHC-b
Glimos for LHC experiments :
G. Benincasa /ATLAS, R. Schmidt /CMS, L. Leistam /Alice, H. Hilke /LHC-b

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Excel table on manufacturers' survey on bromine-free materials also available
but not enclosed, a paper copy can be requested from Reiner Schmidt.