DTBX Electronics Layout

- General layout
- Front End enclosure layout
- HV enclosure layout
- FEB Cooling
- Trigger and Read Out Layout

General DTBX Layout

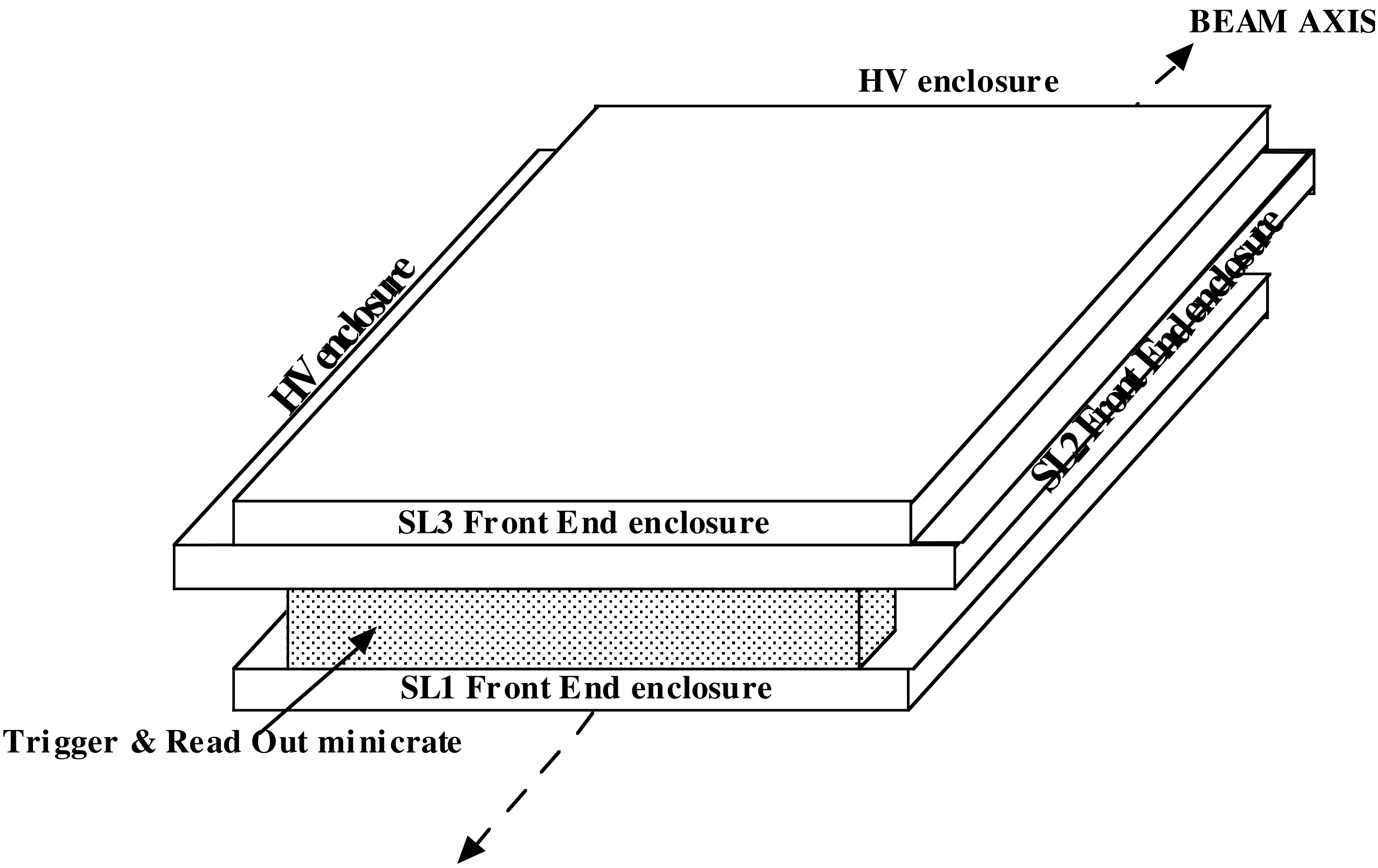


fig.1

- **All the chambers like MB1,MB2,MB3 will have this same structure**
- **In all MB4 chambers, SL2 is substituted by an equivalent thickness of honeycomb**

Front End Enclosure

FE enclosure lodges FE Electronics that consists of two sets of boards forming a sort of sandwich with a 16-ch modularity:

- **the FE board bearing the signal amplifiers, plugged into . .**
- **the High Voltage Coupling board bearing the coupling capacitors for the anode signals.**

- Anode signals are brought into to HVC board via wire connections

- GND by spring contacts grabbing the intermediate aluminium plate

- Signals are received by FEB via a SIL connector and routed to output DIL connector via flat cable

DTBX FE-ENCLOSURE
LAYOUT

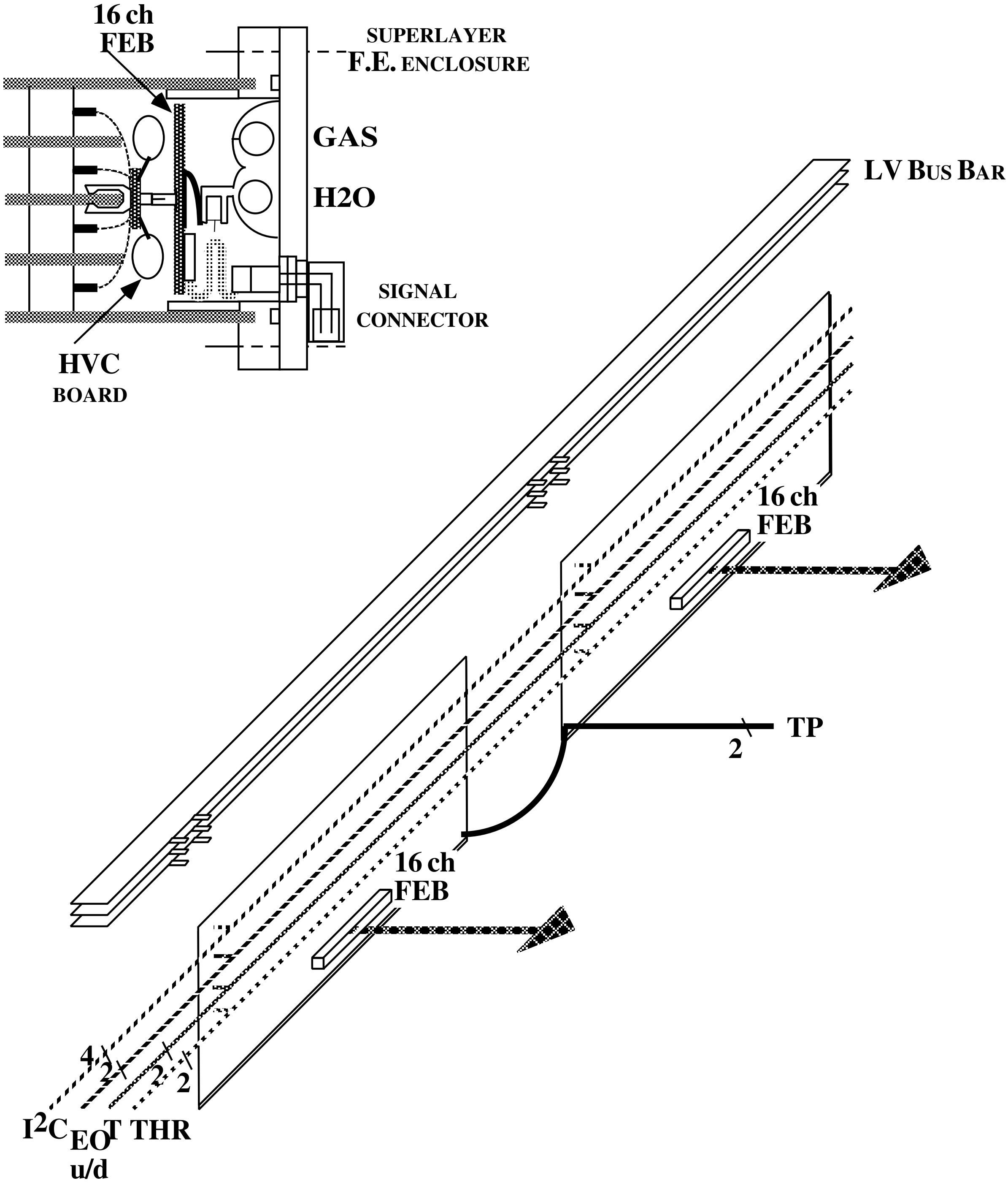


fig.2

- A bus bar provides connection to FEBs for :

- **LV distribution**
- **Threshold and Reference levels**

- A flat cable bus provides connection to FEBs for :

- **I2C local control bus**
- **chip temperature (individual + average)**
- **Test Pulse programming lines**

- Two TP signals per two FEBs are distributed via 50Ω equalised coax lines

- Copper springs along FEB realise both GND and heath sink connection to chamber body by touching a shaped rib of the cover, also lodging the bus bar

- Built in the cover there are two pipes for circulation of cooling water and gas

- Gas flows via a "shower" of tiny holes distributed along the gas pipe

- All connectors for signals and services are lodged onto the FE cover

Front End board & Coupling board

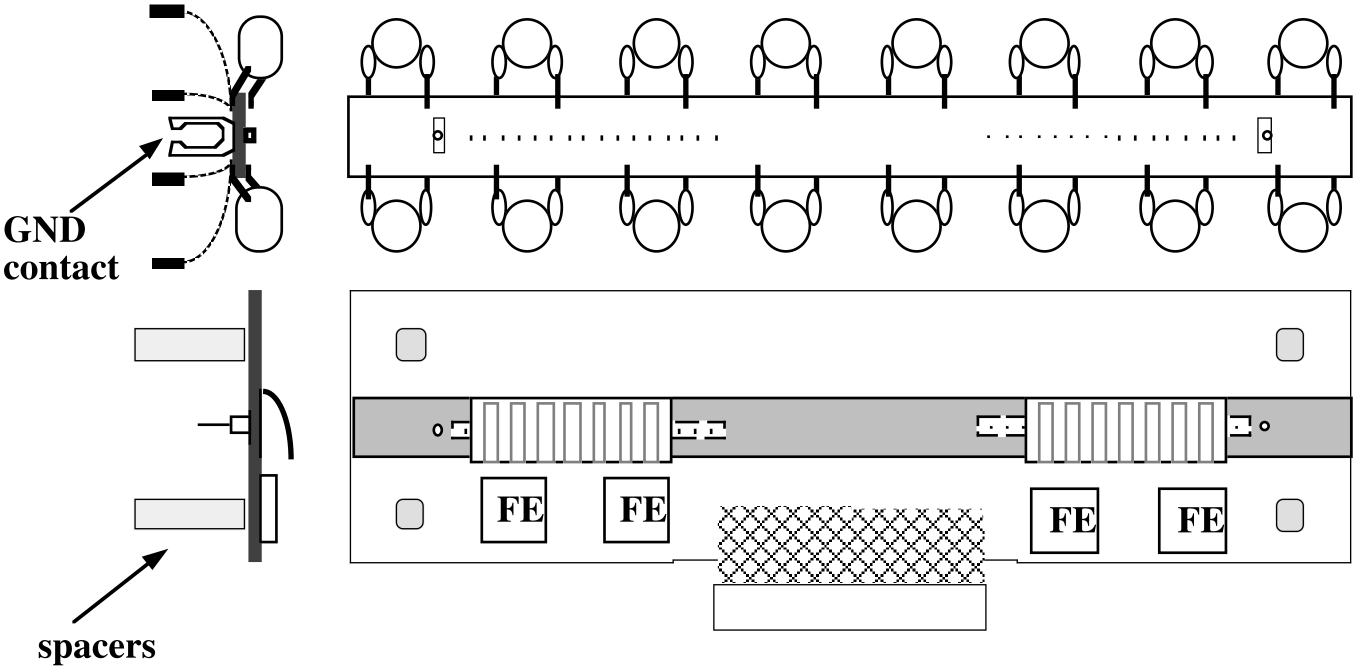


fig.3

Front End Board layout:

- **Layer 1 for Input connections + gnd**
- **Layer 2 for TP distribution in upper part**

  LV distribution in lower part
- **Layer 3 for diffused GND in upper part**

  Output + temperature + Masks in lower part
- **Layer 4 for diffused GND + I^2C bus**

- **Input SIL connections and fixations are in correspondence to GND-heat sink springs, to limit heat flow inwards to the chamber**

<u>High Voltage Coupling board</u>

- The HVC board services 16 channels arranged in 4 ch on 4 layers

- Channel order chosen to ease handling by trigger electronics

- PCB is 4 layers FR4 type:
- **2 inner gnd**
- **1 outer for HV side pads of coupling capacitors**
- **1 outer for LV side paths to single-in-line signal socket**

- signal connections are interleaved to gnd ones to minimise Xtalk

- Four Pin-Guides are foreseen to ease correct insertion of FEB onto HVC

- Coupling capacitors positioned so to ease connections to anode pins

- SMD, 1MΩ resistors referencing LV side signals path to GND

- All HV and LV pads of coupling capacitors isolated with a drop of tyxotropic epoxy glue

- ~40 prototype boards produced and tested since 2 years in MB96 proved adequate *wrt* HV isolation, Xtalk suppression, geometric compatibility and ease of insertion of both wire connections and FEBs

- Only minor changes foreseen to cope with cells exceeding the modularity, at chamber edges.

High Voltage distribution

- The HV distribution is located in the HV enclosure on opposite side of FE enclosure of each SL

- Three HV values are required for chamber operation:

- **-2 kV for Cathodes on I beams**
- **+2 kV for field Strips**
- **+4 kV for anode Wires**

- The following internal segmentation has been chosen:

- **1 HV incoming line per 8 cells for W in a layer**
- **1 HV incoming line per 16 cells for S in a layer**
- **1 HV incoming line per 16 cells for C in a layer**

DTBX HV-ENCLOSURE
LAYOUT

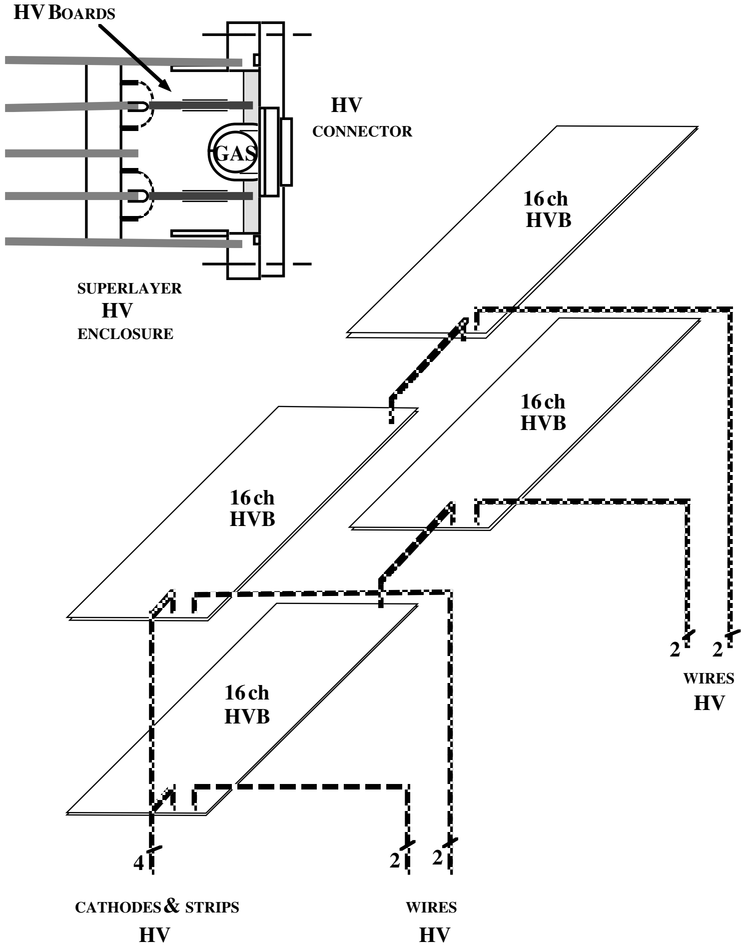


FIG.4

*

Pd 7 mar 97

- The distribution is implemented by means of HV boards accommodating the three voltages for 8 cells in two layers of detector

- HVB are arranged in two raw, servicing two layers each

- Connection to cell electrodes is made via wire connections like as for HVC

- GND connection is assured by spring contacts grabbing the 2nd and 4th aluminium plate, also providing mechanical fixation

- Mechanical fixation is integrated by insulating profiles on the inner cover side

- The cover will lodge two HV 53-pins, custom connectors

- W lines from connector will connect every HVB (1 line per 8 cells)

- S & C lines will connect every 2 HVBs (1 line per 16 cells)

- S & C i/o pins will be jumpered every 2 boards

- The HV side cover integrates the counterpart of the gas shower

High Voltage Board

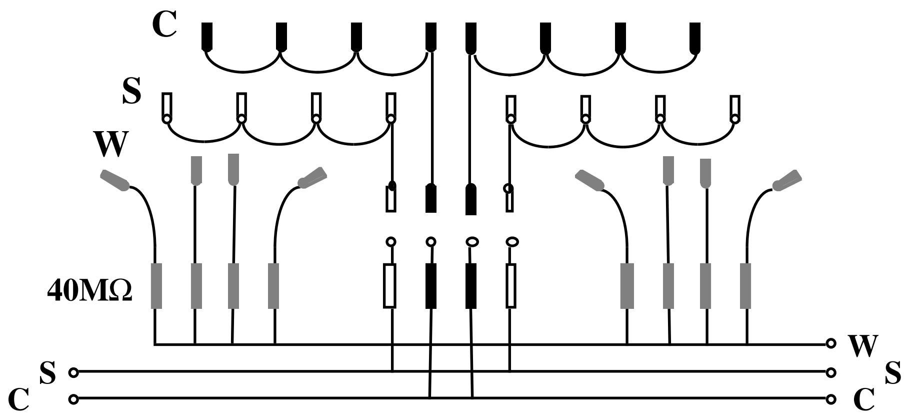
- A HVB consists in a 6 layers FR4 PCB with the following characteristics:

- **1 layer per voltage type for the two cell-layers serviced**
- **2 outermost layers reserved for W anodes**
  2 intermediate layers reserved for Strips
  2 innermost layers reserved for Cathodes
- **layer thickness .5 mm**
- **outer layers covered by .2 mm insulating layer leaving only pads uncovered**
- **diffused ground on every HV layer for shielding and Xtalk control**
- **all soldering pads and pin leads insulated with tyxotropic epoxy glue**
- **points at different voltages distributed so that S voltage is interposed between W and C voltages.**
- **dimensions 305 mm by 35 mm by 3.5 mm**

- The high voltages for W,S & C are brought to the board via the input pins for the 6 layers.

- S &C pins are repeated at both ends of board to allow for two boards to be jumpered; blocking capacitors are provided for all the HV lines

- The incoming HVs are distributed on board through 40 MΩ HV series resistors for each one of the two serviced cell-layers, like in the sketch:



- Resistors are grouped on hybrids and one board is equipped with four hybrids

- The daisy chains are not incorporated in the board and are to be connected to cell electrodes prior to boards' mounting

- About 30 prototype boards have been constructed, tested for several hours in proper gas at +/- 2500 V, +4500 V, and then tested in about a one year operation of MB96 chamber prototype with HV at: +/-1900V, + 3800V

- Currents resulted to be ≤10 nA per board.

Front End Cooling

- A cooling test has been performed on MB96 prototype chamber completely equipped and powered, simulating the worst possible confinement conditions.

- Several temperature probes were located in different places of chamber body, FE -boards and chip-bodies.

- The chamber was powered and let to thermalise, then water flow opened to 1l/min

- Temperature was sampled every one hour, except during the transient, where it was read every 10 minutes

- Ambient day/night oscillations, plus some slower drift due to weather conditions affected input and output water temperatures

- Readings precision of +/- 0.1ºC was rather poor introducing a big error (≈ +/- 20%) on the thermal difference between in and out water (~ 0.5ºC)

Cooling Test setup

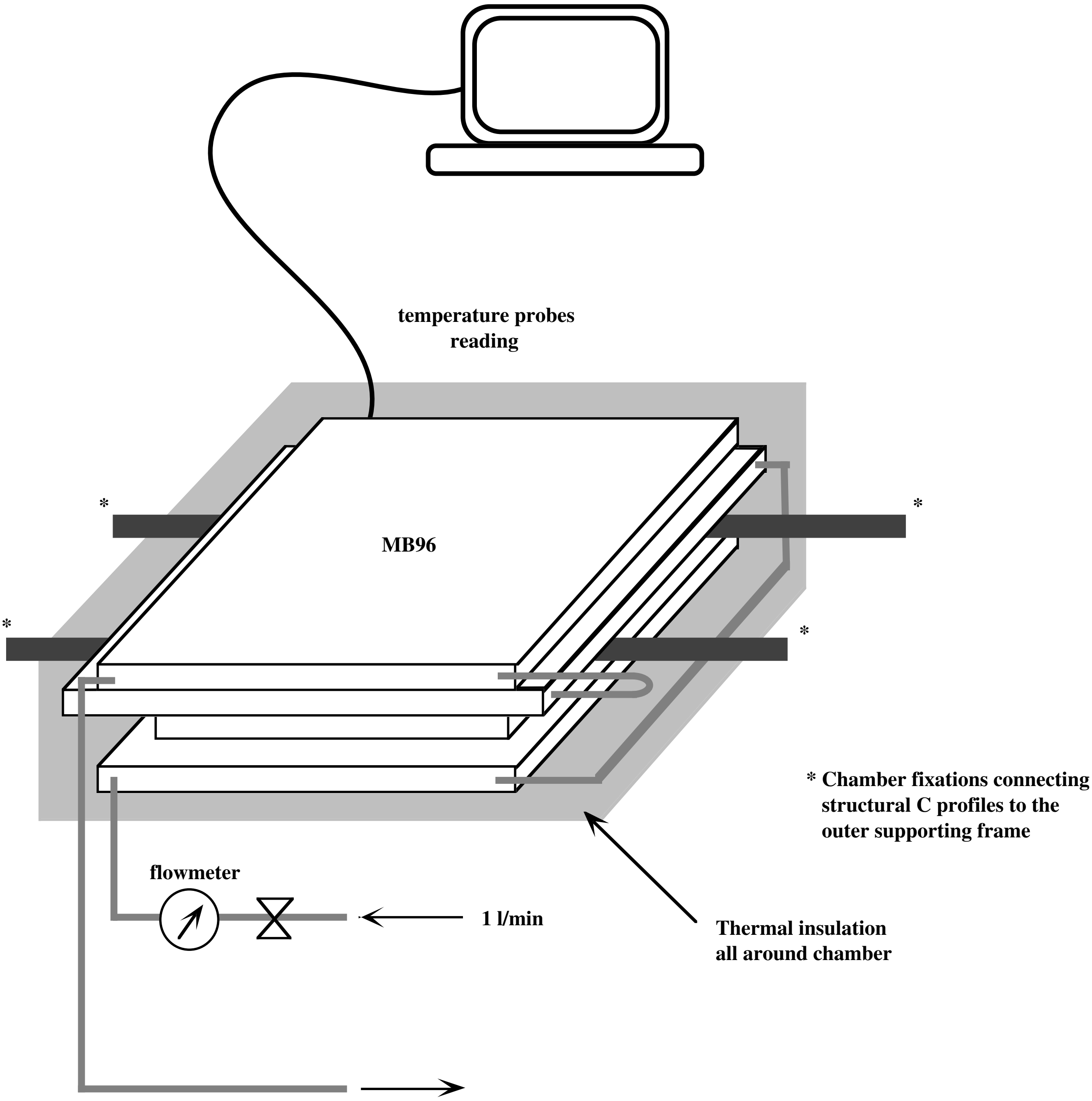


fig. 5

- **FEBs power dissipation: 20W**
- **Fig 6-8 :**

  thermal resistance FEBs to cooling $\vartheta_c \approx$ 8W/^{o}C

- **Fig 8-9-6 (cooling off) :**

  thermal resistance of supports $\vartheta_s \approx$ 5W/^{o}C

- **Fig 8-9-6 (cooling on) : income heat $\approx$ 11.5 W**

$$\Delta T_{i/o} \approx 0.5^oC,\ \Phi = 1\ l/min \Rightarrow$$

- **P_c= 35 W** (.5 *1.7*10^{-2} * 4186) $\approx$ **P_i= 31.5 W into 20%**

Conclusions:

- Taking into account the low level of power dissipated in a chamber (20 ÷ 40 W) and even within the limitations of the measurements, we think we have some sound indications:

- **The integrated thermal contact between FEBs and cooling pipe is more than adequate**
- **The present cooling scheme, within reasonable and safe values of water flow and temperature, can cope with the FEBs power dissipation , being possibly capable of taking away some additional power leaking from ambient**
- **The working temperature of the electronics is largely comfortable accounting for a safe and long lived operation**
- **No appreciable temperature gradient is seen between the heat generation side and the far end of the chamber at thermal equilibrium, so that we can expect negligible mechanical stresses due to thermal gradients, and also uniformity of operation.**

Read Out Status

TDC

- A 32-channel TDC ASIC , developed by CERN/ECP/MIC tested and found to comply with DT requirements
- Present version on 0.7μ technology not appropriate for final solution
- New version under development expected to be ready for production by end 2000

ROB

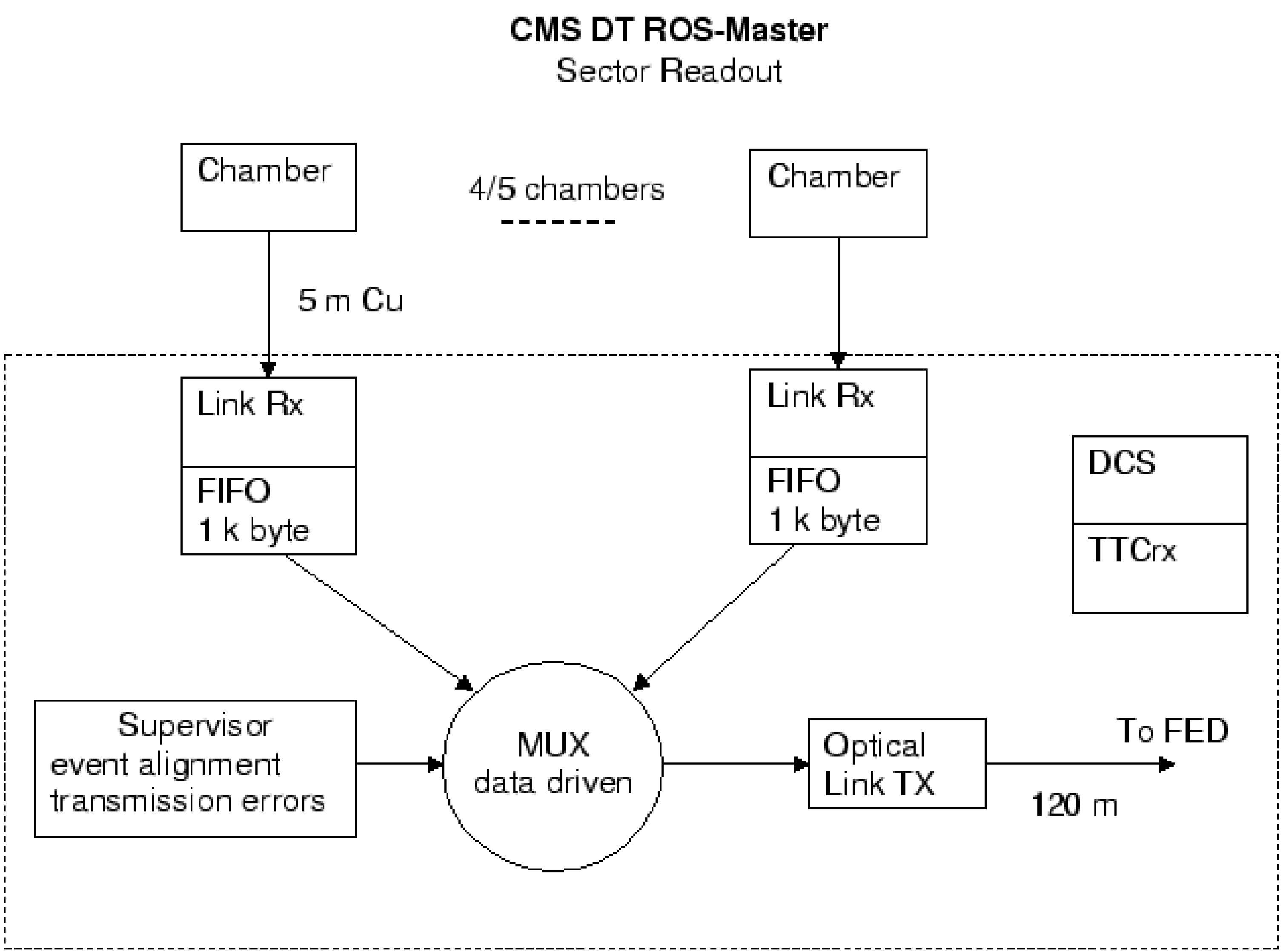
- A full functionality 128-channel Read Out Board prototype has been built and tested on MB96 during 1998 test beam at GIF
  - Preliminary data analysis shows good behaviour of TDCs in real operating conditions, including high background
  - A final version is being designed to be installed on chambers

ROCH

- A chamber server prototype has been built to operate ROB prototypes and used at GIF test
- The final version to be developed during 1999

ROSM

- The ROS Master is now being designed to interface a sector of chambers to DDU on FEDs via opto-link
- The link is expected to be a common solution for CMS


CMS DT ROS-Master
Sector Readout
Chamber
4/5 chambers
Chamber
5 m Cu
Link Rx
FIFO
1 k byte
Link Rx
FIFO
1 k byte
DCS
TTCrx
Supervisor
event alignment
transmission errors
MUX
data driven
Optical
Link TX
To FED
120 m