

BTI REFERENCE MANUAL

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1.0 INTRODUCTION

The trigger front-end device for the DTBX chamber¹ of the CMS muon detector is the "Bunch crossing and Track Identifier" (BTI)². It is an integrated circuit that computes the local muon track parameters and assigns the bunch crossing to it. The best efficiency to noise ratio in the operating background conditions is achievable only with a careful chip setup: the BTI has many programmable parameters like angular acceptance, time filters, drift velocity and wire dead time. The BTI can be programmed either via JTAG chain or via a parallel interface using the trigger data port to propagate trigger parameters from the Trigger Server back to the BTIs through the TRACOs³.

System testability is good owing to built-in self-test logic and JTAG implementation.

2.0 SPECIFICATIONS

The BTI detects, with constant latency, tracks crossing a Superlayer, consisting of four layers of staggered drift tubes, and measures the impact parameters. The BTI, by means of a generalized mean-timer method, is able to identify tracks leaving a signal in a minimum of three out of four tube planes, making its operation tolerant to tube inefficiencies and δ -rays. Each wire signal is stretched in order to consider only single hits in the track-fitting algorithm; when more than one track is recognized in the same bunch crossing cycle, only one is sent to the next trigger preferring clean tracks (four out of four hits).

The CMS trigger requires a position resolution of the order of one millimetre and the best possible angular resolution to reach a good p_T sensitivity for a cut at high momentum⁴ and to reduce the probability of a

¹ F.Gasparini et al, "Performance of a DTBX prototype", Nuclear Instruments and Methods in Physics Research A 344(1994) 137-142

F. Gasparini et al, "Further studies on a DTBX prototype for the CMS muon detector at LHC", Nuclear Instruments and Methods in Physics Research A 360(1995) 507-511.

² M. De Giorgi et al, Efficiency studies of the front-end trigger device of the muon drift tubes for the CMS detector at LHC", Nuclear Instruments and Methods in Physics Research A 398(1997) 203-210.

³ M. De Giorgi et al, "Design and Simulations of the Trigger Electronics for the CMS Muon Barrel Chambers", First Workshop on Electronics for LHC experiments, CERN/LHCC/95-96, October 1, 1995 pg. 222-227.

⁴ A. Kluge et al, "Track Finding Processor in the CMS Muon Trigger", First Workshop on Electronics for LHC experiments, CERN/LHCC/95-96, October 1, 1995

"ghost track" reconstruction. BTI capability to trigger on low p_T muons depends on its angular acceptance

The chamber trigger electronics is designed for high reliability: malfunctioning devices can be easily identified, running built in self tests, and then isolated with only minor and local efficiency losses owing to system redundancy.

3.0 SCHEMATICS

The BTI looks at 9 wires of a Superlayer numbered as shown in Fig.3.0.1. Redundancy is built owing to BTI superposition by 5 cells.

The geometrical angular acceptance of a BTI is

$$\Psi_{geo}^{max} = \tan^{-1} \frac{L_d}{h} = \pm 58^\circ \quad Eq.1$$

where $L_d = 21\text{mm}$ is half the wire pitch and $h = 13\text{mm}$ is the distance between two consecutive wire planes. The device however is fully efficient only up to

$$\Psi_{eff}^{max} = \tan^{-1} \left(\frac{2L_d}{3h} \right) = \pm 47^\circ \quad Eq.2$$

Track whose incident angles are bigger than the value given by Eq.1 are not fully contained in a single BTI; and track angles higher than Eq.2 lead to a poor bunch crossing identification efficiency.

The BTI chip block scheme is shown in Fig.3.0.2.

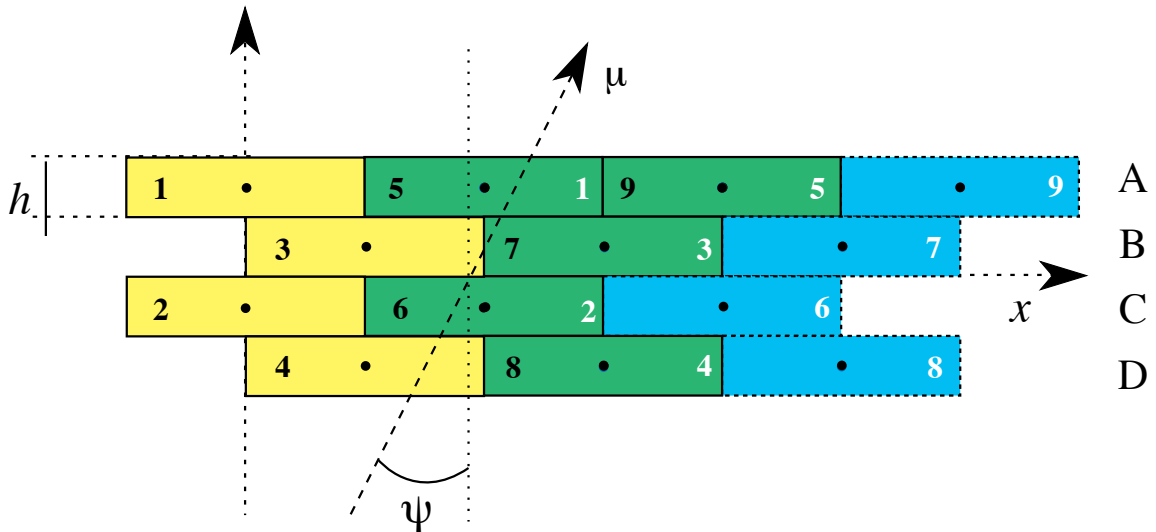


Fig. 3.0.1: Chamber section in the bending plane and BTI allocation. White and black labels refer to superposing BTIs

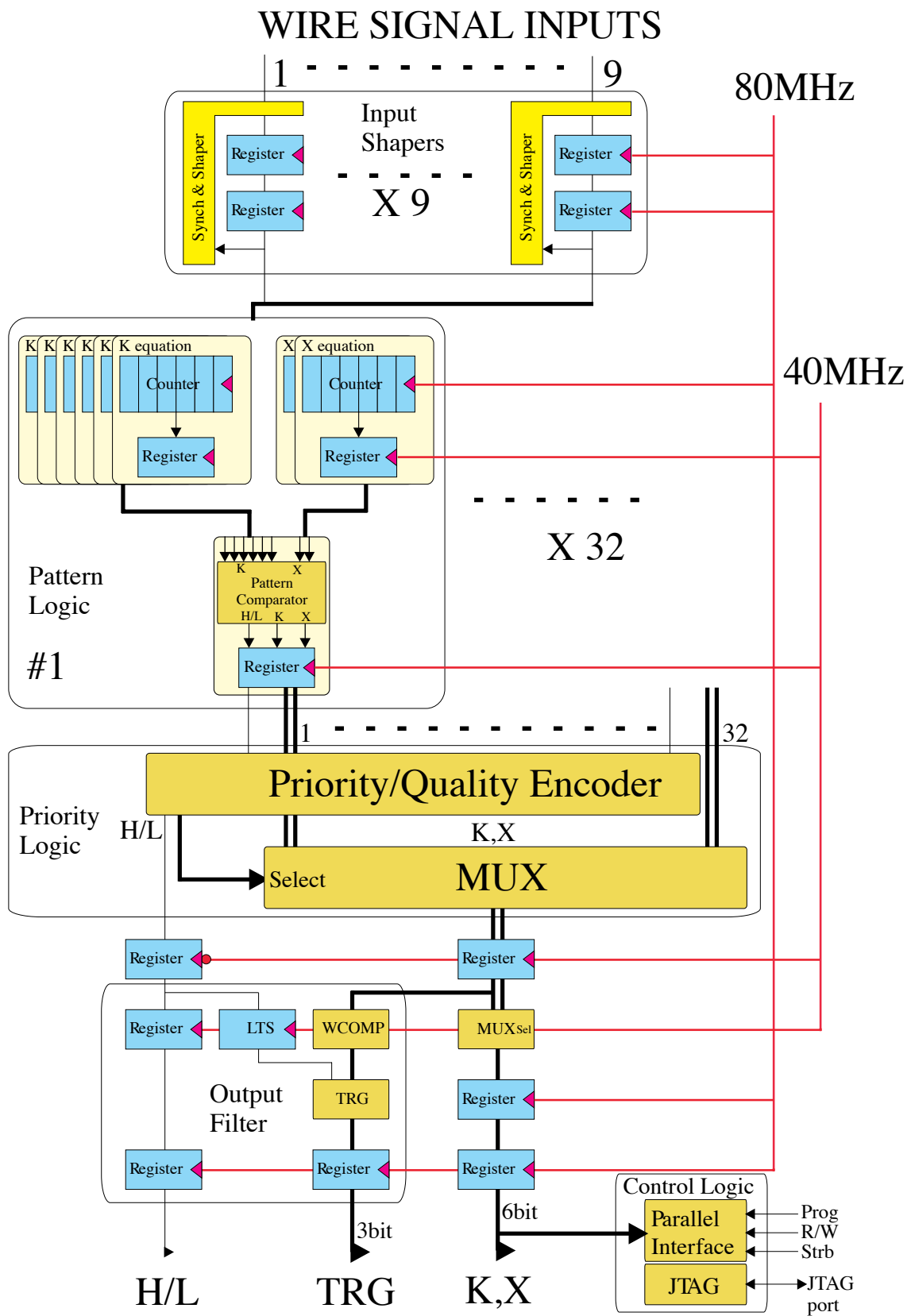


Fig. 3.0.2: BTI block scheme.

$$k = k_g \cdot \tan \Psi + k_0 \quad Eq.3$$

where k_g and k_0 depend on drift velocity:

$$k_g = \frac{h}{v_d \cdot t_{ck}}$$

$$k_0 = \frac{L_d}{v_d \cdot t_{ck}}$$

where v_d is the drift velocity and t_{ck} is equal to 12.5ns. Ψ is the track angle measured from the normal to the chamber. The geometrical meaning of the parameter k is shown in Figure 3.2.1.

The BTI resolution depends on the incident angle and the worst one is obtained for orthogonal tracks, being

$$\Psi_{err}^{max} = \tan^{-1} \left(\frac{v_d \cdot t_{ck}}{h} \right)$$

If D is the track intercept distance, along the plane in the middle of the Superlayer, from the axis of wires 1 and 2, the position equations give an integer parameter x that is the track intercept

$$x = \frac{D}{2v_d \cdot t_{ck}} \quad Eq.4$$

Given a track pattern all the 6 involved wire couples (AB, BC, CD, AC, BD, AD) can give a (k,x) parameter estimation. The 6 k-equations are used to identify the track bunch crossing looking for a coincidence of values, the x-equations are considered only when the alignment of the k-equations is found; therefore only a subset of 2 x-equations per pattern was implemented. If a wire signal is spoiled by a δ -ray or is missing, only 3 out of 6 k-equations will align at the right time giving a low quality trigger. The x-equations (from BC and AD wire couples) will be used depending on the k-equation alignment found, as given in Table 3.2.1.

Track types	X-equation
Clean track	eqAD
A missing	eqBC
B “	eqAD
C “	eqAD
D “	eqBC

Tab 3.2.1: List of x-equation selection rules for all possible track types.

In Fig. 3.2.1 a track crossing the cells of wires 1, 2, 3 and 4 with an angle Ψ and a position x is shown. The estimation of k given by the wire couple 2-3 is

$$Eq_{23}(t) = 2t - (T + ts_3 + ts_2)$$

where t_{s2} and t_{s3} : are the times after the wire signals detection for wires 2 and 3

$$ts_i = t - td_i$$

and T is the maximum drift time.

Equation $Eq_{23}(t)$, evaluated at the right time $t=T$ gives

$$Eq_{23}(T) = td_3 + td_2 - T = k23$$

The same technique applied to all the wire couples, gives the 6 k-equations, measuring the same k-parameter. It can be shown that while the k-equation of a wire couple crossed by the track between the wires is time dependent (increasing or decreasing its value with time) those of wire couples crossed from the same side are time independent giving immediately the k parameter of the track. This is the reason why the BTI track fitting algorithm has a limitation in the angular acceptance: when all tracks pass to the right or to the left of the wires the BTI is not able to identify anymore the parent bunch crossing. This happens also for some trigger patterns where one tube plane is not considered; these patterns are called x-patterns and are disabled unless the flag XON is set high.

Similar equations can be written for the x parameter. Appendix B gives the description of all the implemented k-equations and x-equations.

3.3 Pattern Recognition

Track pattern validation (see the pattern list in Appendix C) and the identification of the parent bunch crossing are performed by this block. Every pattern block looks for a matching of the angles given by 6 equation counters called eqAB, eqBC, eqCD, eqAC, eqBD and eqAD where the letters A,B,C and D can be replaced by the wire number of the relative plane in the Superlayer.

Each equation is matched to eqAD, since this one is giving the best determination of the k-parameter, due to its larger lever arm. The matching tolerance of eqAB, eqBC and eqCD has a programmable acceptance (see the use of ACx parameters in paragraph 4.0: Internal Register Files) while the matching tolerance of eqAC and eqBD is fixed to ± 1 . When all the 5 equation values match with eqAD within the given acceptance a high quality trigger (HTRG) is generated with angle and position values. It might happen that only three wire planes give a clean signal, due to a missing or spoiled wire signal. If wire plane A cannot be considered, eqAB, eqAC and eqAD are no more valid; the matching can be found only between eqBC, eqCD and eqBD where the last one is giving the best k-parameter estimation. Table 3.3.1 shows the k-equation comparison scheme implemented for all the possible track types.

Track types	eqAB	eqBC	eqCD	eqAC	eqBD	eqAD
Clean track	x	x	x	x	x	Ref
A missing		x	x		Ref	
B "			x	x		Ref
C "	x				x	Ref
D "	x	x		Ref		

Tab 3.3.1: Matching scheme of the k-equations for all possible track types (Ref is the reference couple).

Every time only 3 out of 6 equations match, a low quality trigger (LTRG) is given. The use of a quality bit (H/L pin) allows the next device in the trigger chain to distinguish between clean tracks and potentially wrong triggers. Low quality triggers are mainly due to virtual tracks, called "ghost tracks": out of time alignments due to the left/right ambiguity of the drift cell.

3.4 Pattern Selection

If several track patterns give a trigger at the same time, only one is selected preferring a high quality track. If the pattern quality is the same an encoded preference order is used.

3.5 LTS Filter and Angle Window Comparator

The capability to trigger on "dirty" tracks (three out of four aligned hits) causes the BTI to trigger frequently at the wrong time, either before or after the right trigger time, even processing a clean track. The phenomenon, called "ghost track" generation, is the main source of trigger noise.

The "ghosts" production is a purely geometrical mechanism, due to the left-right ambiguity (see Fig. 3.5.1): when a track signal is detected at the BTI input, the drift direction is unknown. In order to be efficient, and to be able to trigger even if only three out of four hits are good, all the combinations and possibilities must be evaluated at the same time. This makes the right trigger output of a clean track to be associated with a mean value of 3 low quality triggers associated to "ghost tracks". These wrong triggers are distributed in time around the right one in the range of $\pm 8bx$. In the example shown in Fig. 3.5.1 a clean straight track has two associated ghosts. The first (ghost #1) is generated assuming that the signal coming from wire 2 has been spoiled by a δ -ray. The second one (ghost #2) is generated considering that the signal from wire 5 could be missing because of a local inefficiency.

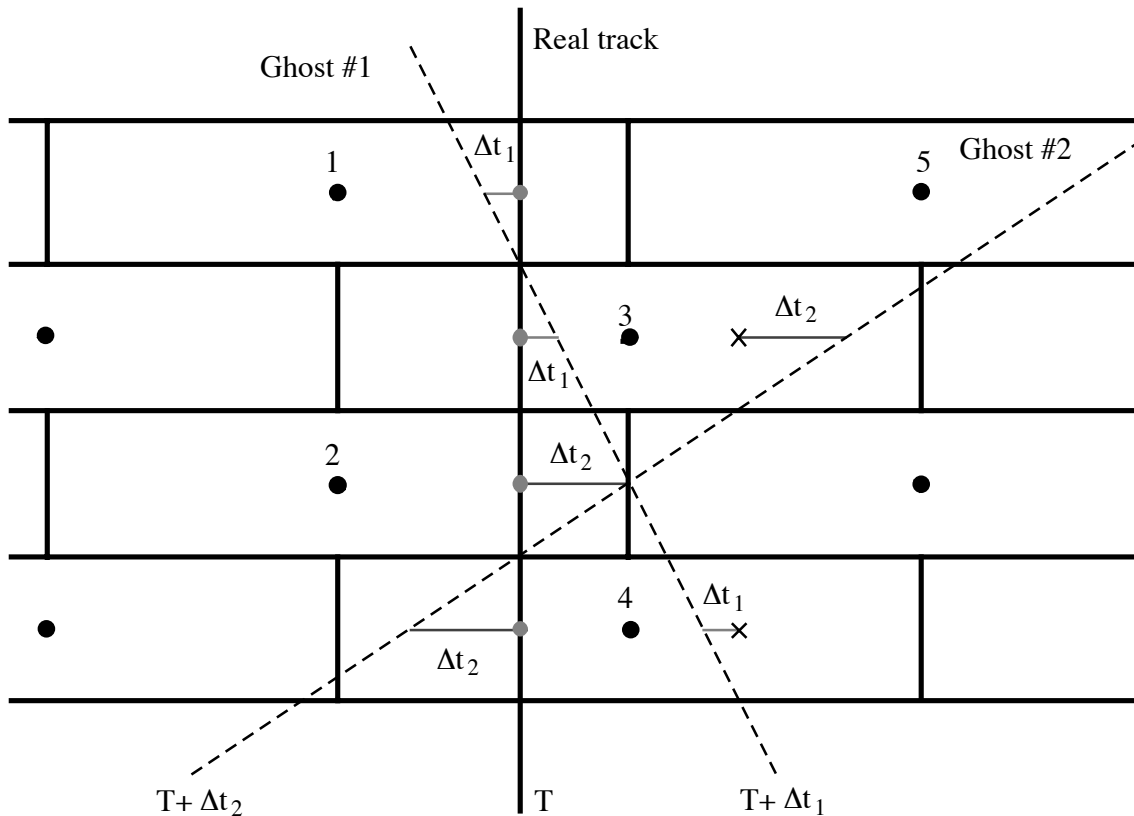


Fig. 3.5.1: "Ghost tracks" generation example.

In order to reduce the number of "ghost" triggers, the cancellation of low quality triggers in the range $(-1bx, +8bx)$ about a high quality trigger is very efficient and latency inexpensive; this Low Trigger Suppression filter is programmable (LTS and SET registers).

As described elsewhere³ each BTI of the chamber outer Superlayer is interfaced to three Track Correlators (TRACO). In order to reduce the probability to generate multiple triggers from single tracks, an angular filter has been included in order to send to each TRACO only those tracks that could be fully contained in it. The trigger strobe is split into three signals, one for each TRACO, activated only if the track angle is within the associated programmable window. Quality bit and angle/position lines are common to the three TRACOs. The BTI trigger output bus consists of the three trigger stobes TRGL, TRGC, TRGR, the quality bit H/L and the data bus AP<5:0> where angle and position are multiplexed at 80MHz.

3.6 Control Logic

This block contains a JTAG⁶ interface and a bidirectional parallel interface. The JTAG port (tms, tck, tdi, tdo) can be used either to control chip interconnections or to program internal registers. An additional capability of this interface is the monitoring of chip activity without interfering with the trigger function. This can be performed simply

⁶ IEEE Std 1149.1-1990 "IEEE Standard Access Port and Boundary-Scan Architecture", May 21, 1990

reading the snap registers connected to the input signals and to the output bus (see snap registers description in the next section).

The parallel interface, much faster than the JTAG port, can program all the BTI internal registers and is used only as a backup solution for BTI access. Using the angle/position trigger bus as data bus the TRACO has the possibility to access the internal registers of the connected BTIs and downstream the Track Server Sorter (TSS) can access all chamber TRACOs. Associating a specific address to the BTI input port (WIN) data can be exchanged with the front-end electronics as described in 6.0: Parallel Interface.

3.7 Reset Logic

At power on all chips can be put in a default state using the asynchronous reset line HRSTB. The synchronous reset (SYRSB) can be used to clear all internal registers with the exception of the configuration parameter register file.

An additional synchronous reset command (SNRSB) clears only the snap registers.

4.0 INTERNAL REGISTER FILES

BTI registers are grouped into 4 files of 6 bit words accessible using dedicated JTAG instruction addresses: configuration, test, snap and boundary.

4.1 Configuration

This register file collects all the set up registers for the BTI trigger operation and has to be programmed after a power-on reset (HRSTB low):

- ST43 and RE43 are programmed to set the drift velocity from 44.4 to 66.7 $\mu\text{m}/\text{ns}$ as described in Appendix D.
- WEN is the input wire mask register (one bit per wire): when a bit is set low it disables the corresponding wire input.
- DEAD is the wire dead time that should be set as suggested in Appendix D in order to maximise the efficiency/noise ratio.
- LH, LL are the angular window limits for the left TRACO (interested to negative track angles): a "left trigger" output (LTRG) is generated when:

$$LL \leq \text{track angle} \leq LH$$

CH, CL and RH, RL are the angular limits respectively for the centred TRACO and for the TRACO to the right.

- TSTON, TEST and TEN are flags used for BTI self test purposes as described in 8.0: Test and Debug Features.

Add	b5 (MSB)	b4	b3	b2	b1	b0 (LSB)
0	st43<5>	st43<4>	st43<3>	st43<2>	st43<1>	st43<0>
1	re43<1>	re43<0>	-	wen<9>	wen<8>	wen<7>
2	wen<6>	wen<5>	wen<4>	wen<3>	wen<2>	wen<1>
3	dead<5>	dead<4>	dead<3>	dead<2>	dead<1>	dead<0>
4	lh<5>	lh<4>	lh<3>	lh<2>	lh<1>	lh<0>
5	ll<5>	ll<4>	ll<3>	ll<2>	ll<1>	ll<0>
6	ch<5>	ch<4>	ch<3>	ch<2>	ch<1>	ch<0>
7	cl<5>	cl<4>	cl<3>	cl<2>	cl<1>	cl<0>
8	rh<5>	rh<4>	rh<3>	rh<2>	rh<1>	rh<0>
9	rl<5>	rl<4>	rl<3>	rl<2>	rl<1>	rl<0>
10	tston	test	ten	-	xon	ron
11	set<2>	set<1>	set<0>	lts<1>	lts<0>	-
12	ac1<1>	ac1<0>	ac2<1>	ac2<0>	acl<1>	acl<0>
13	ach<1>	ach<0>	-	-	-	-

Tab 4.1.1: Configuration register file.

- XON is a flag activating the x-patterns: the low quality track patterns associated to tracks passing on the same side of the three wires. Setting XON high enables the x-patterns and rises the efficiency but more out of time triggers are generated, being the time resolution of x-patterns intrinsically poor and dependent on track impact parameters.

- RON flag enables the redundant patterns, i.e. the ones already covered by the neighbouring BTIs. Setting RON high the BTI extends its acceptance range to recover part of a neighbouring BTI inefficiency, or to optimise geometric acceptance (if the BTI is the last one).

- AC1, AC2, ACH and ACL allow to program part of the alignment acceptance of equation counters in the track pattern blocks. The track patterns look for an equation counter matching (see Appendix C) with default tolerances set depending on equation and on pattern. Some pattern is critical from the noise point of view or too much sensitive to drift cell nonlinearity as in the case of patterns triggering only on large angle tracks. For this reason the default maximum alignment error of 2 between eqAB, eqBC and eqCD with respect to eqAD can be overwritten using the ACx parameters as described in Table 4.1.2.

ACx	Matching of eqX and eqAD
00	$eqX-1 \leq eqAD \leq eqX+1$
01	$eqX \leq eqAD \leq eqX+2$
10	$eqX-2 \leq eqAD \leq eqX$
11	$eqX-2 \leq eqAD \leq eqX+2$

Tab 4.1.2: Equation alignment programmable tolerance.

The section 7.0: Operating Instructions gives more information about the use of these parameters.

4.2 Test

This register file (Tab. 4.2.1) is mainly used to run self-tests of the BTI but can be used also to mask specific track patterns:

- PTMS is the track pattern mask. A pattern is disabled if the correspondent bit is set low.
- TCEN is the equation counter group test enable and is used only for chip validation as described in section 8.0: Test and Debug Features.
- WD1 ÷ WD9 are the drift time registers used to emulate a track. WD1 is the drift time in 12.5ns units for the signal of wire 1; when set to zero it gives no signal. The section 8.0: Test and Debug Features gives more information about track emulation procedure.

4.3 Snap

This register file (Tab. 4.3.1) is used for chip monitoring purposes:

- SNW is the snap register of the input wires: a bit is set high when the correspondent wire is hit by a track.
- LPOS and LANG are position and angle of the first low quality trigger given from the BTI after the last reset.
- In LQTR are stored LTRG (bit 2), CTRG (bit 1) and RTRG (bit 0) of the first low quality trigger given from the BTI after reset time.
- HPOS and HANG are position and angle of the first high quality trigger given from the BTI after reset time.

Address	b5	b4	b3	b2	b1	b0
14	-	-	-	-	ptms<31>	ptms<30> >
15	ptms<29>	ptms<28>	ptms<27>	ptms<26>	ptms<25>	ptms<24> >
16	ptms<23>	ptms<22>	ptms<21>	ptms<20>	ptms<19>	ptms<18> >
17	ptms<17>	ptms<16>	ptms<15>	ptms<14>	ptms<13>	ptms<12> >
18	ptms<11>	ptms<10>	ptms<9>	ptms<8>	ptms<7>	ptms<6>
19	ptms<5>	ptms<4>	ptms<3>	ptms<2>	ptms<1>	ptms<0>
20	tcen<11>	tcen<10>	tcen<9>	tcen<8>	tcen<7>	tcen<6>
21	tcen<5>	tcen<4>	tcen<3>	tcen<2>	tcen<1>	tcen<0>
22	wd1<5>	wd1<4>	wd1<3>	wd1<2>	wd1<1>	wd1<0>
23	wd2<5>	wd2<4>	wd2<3>	wd2<2>	wd2<1>	wd2<0>
24	wd3<5>	wd3<4>	wd3<3>	wd3<2>	wd3<1>	wd3<0>
25	wd4<5>	wd4<4>	wd4<3>	wd4<2>	wd4<1>	wd4<0>
26	wd5<5>	wd5<4>	wd5<3>	wd5<2>	wd5<1>	wd5<0>
27	wd6<5>	wd6<4>	wd6<3>	wd6<2>	wd6<1>	wd6<0>
28	wd7<5>	wd7<4>	wd7<3>	wd7<2>	wd7<1>	wd7<0>
29	wd8<5>	wd8<4>	wd8<3>	wd8<2>	wd8<1>	wd8<0>
30	wd9<5>	wd9<4>	wd9<3>	wd9<2>	wd9<1>	wd9<0>

Tab 4.2.1: Test register file.

- In HQTR are stored LTRG (bit 2), CTRG (bit 1) and RTRG (bit 0) of the first high quality trigger given from the BTI after reset time.

- RE23, ST2, ST ÷ ST7 are the internally calculated drift velocity parameters as given in Appendix D. In particular ST is the maximum drift time expressed as number of CK cycles (12.5ns), normally ranging from 26 to 36.

The snap registers are cleared by a SNPRST signal and are written only once, after the first trigger occurrence.

Address	b5	b4	b3	b2	b1	b0
31	-	-	-	snw<9>	snw<8>	snw<7>
32	snw<6>	snw<5>	snw<4>	snw<3>	snw<2>	snw<1>
33	-	-	-	lqtr<2>	lqtr<1>	lqtr<0>
34	lpos<5>	lpos<4>	lpos<3>	lpos<2>	lpos<1>	lpos<0>
35	lang<5>	lang<4>	lang<3>	lang<2>	lang<1>	lang<0>
36	-	-	-	hqtr<2>	hqtr<1>	hqtr<0>
37	hpos<5>	hpos<4>	hpos<3>	hpos<2>	hpos<1>	hpos<0>
38	hang<5>	hang<4>	hang<3>	hang<2>	hang<1>	hang<0>
39	re23<1>	re23<0>	st23<4>	st23<3>	st23<2>	st23<1>
40	st23<0>	st<5>	st<4>	st<3>	st<2>	st<1>
41	st<0>	st2<6>	st2<5>	st2<4>	st2<3>	st2<2>
42	st2<1>	st2<0>	st3<6>	st3<5>	st3<4>	st3<3>
43	st3<2>	st3<1>	st3<0>	st4<7>	st4<6>	st4<5>
44	st4<4>	st4<3>	st4<2>	st4<1>	st4<0>	st5<7>
45	st5<6>	st5<5>	st5<4>	st5<3>	st5<2>	st5<1>
46	st5<0>	st7<7>	st7<6>	st7<5>	st7<4>	st7<3>
47	st7<2>	st7<1>	st7<0>	-	-	-

Tab 4.3.1: Snap register file

4.4 Boundary Scan

This register file (see Tab. 4.4.1) is accessible via JTAG and is used only for Trigger board connectivity tests.

5.0 JTAG INTERFACE

The JTAG⁷ port is available for interconnection testing and for BTI registers programming. The implemented instructions are the mandatory Extest, Bypass and Sample, and the dedicated Config, Test and Snap as described in Tab. 5.0.1.

The first one (Extest) is used for PCB testing and in general for system interconnect verification. This function allows to write in all chip outputs a value and to verify that the same pattern can be received at the inputs of downstream connected devices.

The bypass instruction is used to skip a device in the JTAG chain.

Sample instruction can be used to read BTI periphery without interfering with chip operation.

Dedicated instructions are used to access Configuration, Test and Snap register files.

IN	bit	description
w<9:1>		wire inputs
ferdb		Front-end read strobe
fewrb		Front-end write strobe
prgb		Parallel interface enable
strb		Parallel interface data strobe
rwb		Parallel interface read/write
trg<2:0>	2	Right trigger
	1	Center trigger
	0	Left trigger
hlb		Trigger quality
trgoeb		Trigger output enable
d<5:0>	5	Parallel interface data bus
ap<5:0>	5	Trigger angle/position bus
apoeb		Trigger apd bus enable

Tab 4.4.1: Boundary register file.

6.0 PARALLEL INTERFACE

The BTI registers can be programmed very efficiently through a parallel interface. This port is controlled by three input lines: PRGB,

Instruction	Name	Description
0	EXTEST	Boundary scan test
1	-	-
2	SAMPLE	Chip boundary sampling
3	-	-
4	-	-
5	-	-
6	-	-
7	CONFIG	Configuration register file
8	TEST	Test register file
9	SNAP	Snap register file
10	-	-
11	-	-
12	-	-
13	-	-
14	-	-
15	BYPASS	Chip bypassing

Tab 5.0.1: JTAG instruction set.

STRB and R/W. The I/O data bus uses the same set of pins as the angle/position 6 bit trigger bus. As shown in Fig.6.0.1 a low level on PRGB turns on the interface and prevents any trigger data to be generated. The internal registers can be accessed randomly or sequentially.

After PRGB is pulled low the first input word is the address pointer and the second one is to read or write operation into the data register. If PRGB is kept low the address pointer is self-incremented and another datum can be read or written into the next register. When PRGB goes high the address pointer is cleared.

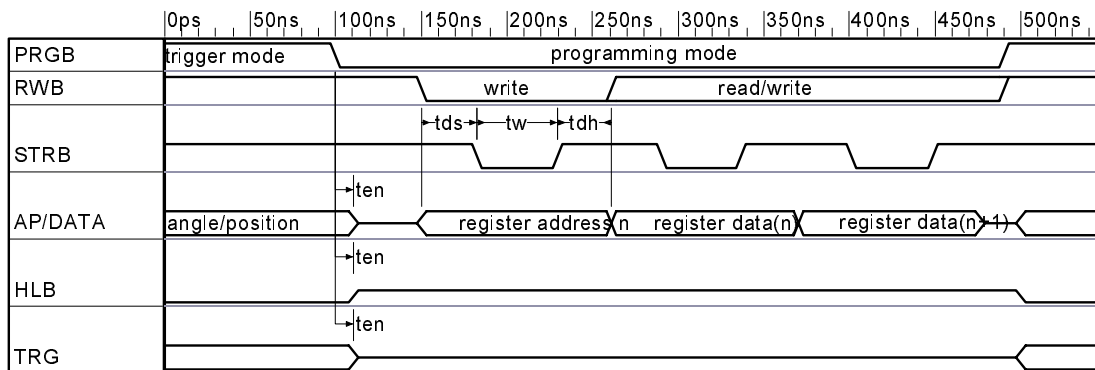


Fig. 6.0.1: Parallel Interface access timing.

6.1 Front-end interface

The backpropagation of the programming data using the parallel interface can go up to the front-end logic passing through the BTI's Front-end Interface.

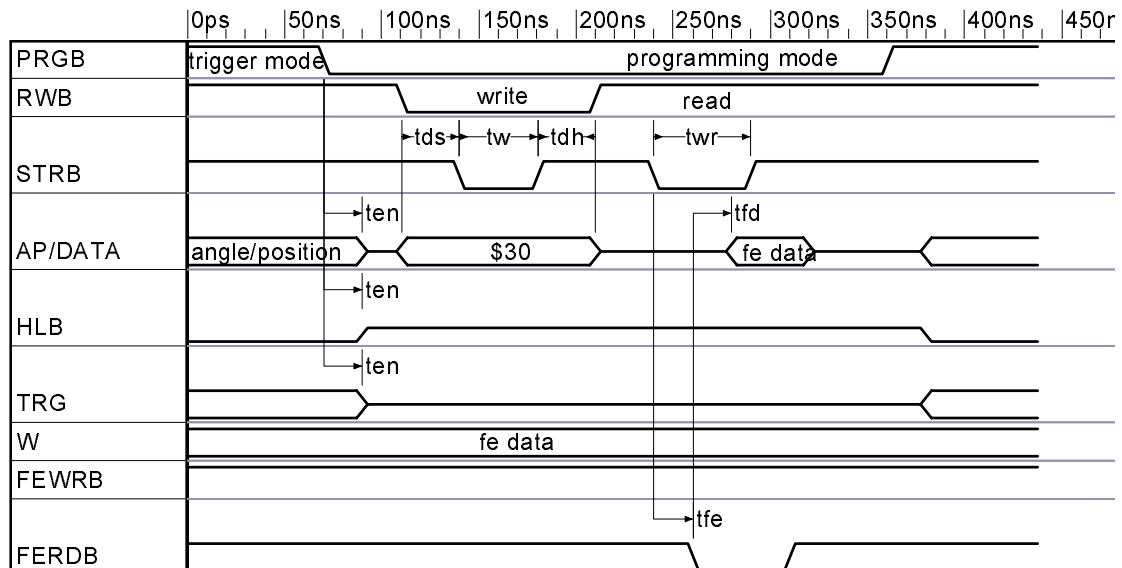


Fig. 6.1.1: Front-end Parallel Interface read operation.

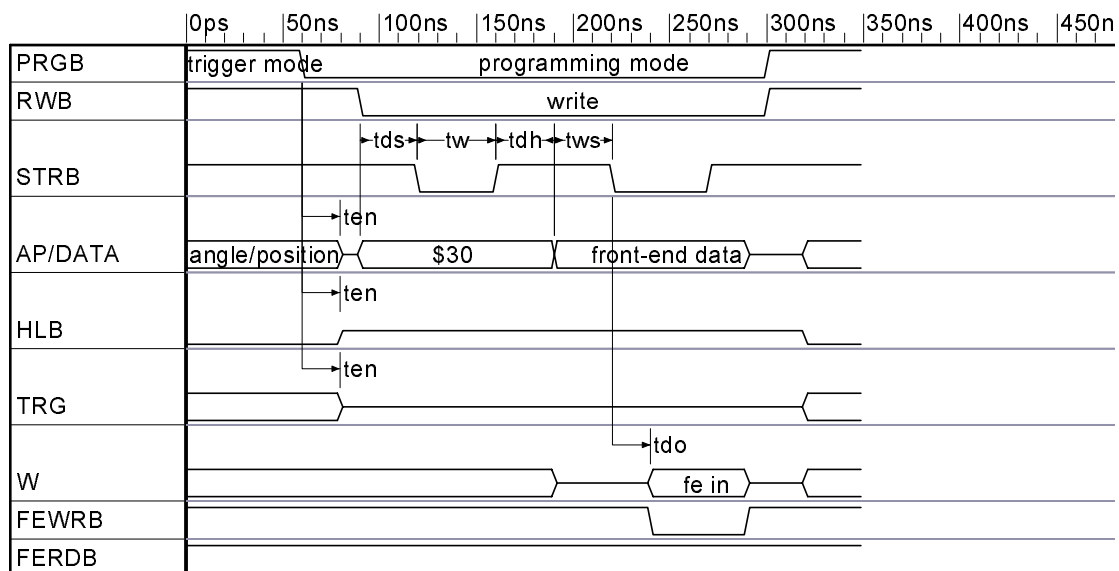


Fig. 6.1.2: Front-end Parallel Interface write operation.

The communication protocol, as shown in Fig.6.1.1 and 6.1.2 is simple: when the BTI is addressed (PRGB low) it is possible to connect the “wire port” (WIN bus) to the angle/position port (AP bus) in both directions.

The address of the “wire port” is 48 and it can be read or written in the same way the other registers are. A read or write operation performed at this address generates a FERDB (front-end read strobe) or FEWRB (front-end write strobe) strobe signal.

7.0 OPERATING INSTRUCTIONS

BTI operations start at power on with a hardware reset command, executed pulling low HRSTB. While CK and PHI are running, the synchronous reset command SYRSB can be used to clear the internal registers with the exception of the configuration register file.

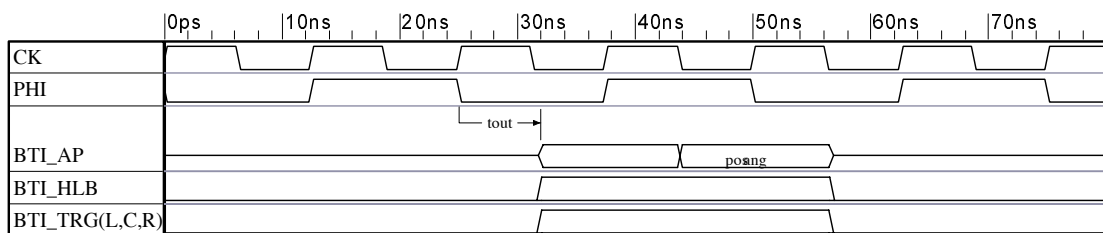


Fig. 7.0.1: BTI output timing.

A dedicated synchronous reset (SNRSB) is available to clear only the snap register file and this operation does not interfere with the triggering function.

CK and PHI are respectively the sampling clock and the output clock. The latched input signals coming from WIN are sampled at the rising edge of CK while trigger angle data are output at the falling edge of PHI (see the timing diagram of Fig.7.0.1). The angle value is given first (during the low phase of PHI) and then the position is output during the high phase of PHI. It is foreseen that angle/position values are sampled by TRACOs on the rising/falling edge of PHI respectively, while trigger strobes and quality bit are sampled on the rising edge of PHI. In order to enable the trigger data bus, PRGB must be high.

The BTI output is meaningless for the first 20 PHI cycles after an hardware reset (HWRST low).

The BTI trigger set-up is described in the next four steps.

7.1 DRIFT CELL PARAMETERS

The drift velocity is the fundamental parameter of the BTI. This parameter is coded, in order to simplify internal calculations, as described in Appendix D. Once the drift velocity is measured the internal registers ST43, RE43 and DEAD must be programmed accordingly.

	1L1 patterns					1H1 patterns				
Eq	-2	-1	0	1	2	-2	-1	0	1	2
AB		x	x	x			x	x	x	
BC	x	x	x					x	x	x
CD		x	x	x			x	x	x	
AC		x	x	x			x	x	x	
BD		x	x	x			x	x	x	
	L11 patterns					H11 patterns				
Eq	-2	-1	0	1	2	-2	-1	0	1	2
AB	x	x	x					x	x	x
BC		x	x	x			x	x	x	
CD		x	x	x			x	x	x	
AC		x	x	x			x	x	x	
BD		x	x	x			x	x	x	
	11L patterns					11H patterns				
Eq	-2	-1	0	1	2	-2	-1	0	1	2
AB		x	x	x			x	x	x	
BC		x	x	x			x	x	x	
CD	x	x	x					x	x	x
AC		x	x	x			x	x	x	

Tab. 7.3.1: Equation alignment acceptance mask for Normal and Critical patterns: the equation counters are considered aligned if the difference with respect to the EqAD is within the specified limits.

A high quality trigger for normal patterns is recognised when equation counters AB, BC and CD differ from AD within ± 2 and AC, BD differs from AD within ± 1 . For critical patterns the AB, BC and CD equation counters have half the normal error tolerance, i.e. ± 1 referred to EqAD. Unfortunately these critical patterns are mainly looking for high angle tracks where the relation between distance from the wire and drift time of a cell is not linear any more.

An effective way to reduce the drift time distortion at high angle has been found applying an offset to the alignment of eqAB, eqBC and eqCD with respect to eqAD as shown in table 7.3.2. Appendix C gives the list of patterns and the respective pattern type.

Track patterns have been grouped in classes with different choices of alignment acceptance for equation counters AB, BC and CD. Four different kinds of alignment acceptances have been defined, associated to four programmable parameters: AC1, AC2, ACH and ACL. The possible alignment acceptances are given in Table 7.3.3. If ACx is equal to 0 a tolerance of ± 1 is allowed; if ACx is equal to 1 or 2 the tolerance is still ± 1 but an offset is applied of +1 or -1 respectively. If ACx is equal to 2

the standard alignment tolerance of ± 2 is applied. Each track pattern type (normal, 1L1, etc.) refers to a specific combination of ACx for the acceptance of equations AB, BC, CD; the corresponding acceptances are given in Tab. 7.3.3. Standard programming values for ACx are given in Tab. 7.3.4.

ACx	-2	-1	0	1	2
00		x	x	x	
01			x	x	x
10	x	x	x		
11	x	x	x	x	x

Tab. 7.3.3: ACx parameter coding for equation alignment acceptance.

AC1	00
AC2	11
ACH	01
ACL	10

Tab. 7.3.4: Default track pattern acceptance parameters.

The default settings can be changed: for example when all the ACx parameters are equal to the binary value 11 the alignment acceptance is the maximum possible (± 2) giving the highest probability to trigger on distorted tracks.

8.0 TEST AND DEBUG FEATURES

The BTI chip has a built in self-test logic aiming to minimise the number of vectors needed for chip validation. Validation mode can be activated programming flags VAL and TSTON, as explained in detail in Appendix E.

Snap registers, connected to input wire signals and output trigger data are provided for online trigger system monitoring via JTAG interface. The input wire snap flip-flops are set when a signal has been received by the BTI after the last reset (SNRSB). The output trigger data snap registers keep the full trigger information: LTRG, CTRG, RTRG, H/L, ANG<5:0> and POS<5:0> either for the first low quality trigger occurred or the first high quality trigger generated after the last reset.

Another feature implemented for test purposes is the possibility to disconnect by software the BTI from the chamber and to use internal programmable delays as drift cell emulators. Setting high the TEN flag makes the wire inputs WIN to be inactive. The internal registers

WD1<5:0> to WD9<5:0> are the starting values of drift time counters. In order to emulate an event, first the WDX registers are set equal to the drift times (in 12.5ns steps) associated to the track. When TSTON is set high, the drift counters start counting down, simulating the track signal generation (when WDn<5:0> is set to zero the relative wire doesn't give any signal). This capability to simulate real tracks can be used on the field to test the trigger chain in special situations.

APPENDIX A: TECHNICAL SPECIFICATIONS

A1: Features

- . Operating voltage $3.3V \pm 0.3V$
- . TTL/CMOS compatible inputs
- . Operating speed 40MHz (80MHz WIN sampling)
- . Low power 0.5_μ CMOS process
- . JTAG interface
- . Parallel interface
- . Emulation and monitoring features
- . High drive capability: 6.5ns @ 150pF
- . TQFP 64 pin production package
- . PLCC 64 pin prototype packaging

A2: BTI PLCC64 pinout

Pi n	Name	Type	Pin	Name	Type
1	CK	In + pulldown	35	TMS	In Schmitt + pullup
2	Vss	Periphery DC	36	TDI	In Schmitt + pullup
3	Vdd	Periphery DC	37	TDO	Out 3-State + pullup
4	SNPRST	In Schmitt + pullup	38	STRB	In Schmitt + pullup
5	Vdd	Periphery AC	39	RWB	In Schmitt + pullup
6	Vss	Core	40	HLB	Out 3-State + pulldown
7	Vdd	Core	41	Vss	Periphery AC
8	Vss	Periphery AC	42	Vss	Periphery AC
9	Vss	Periphery DC	43	Vss	Periphery DC
10	nc		44	nc	
11	Vss	Core	45	Vss	Core
12	Vss	Periphery AC	46	Vss	Periphery AC
13	WIN<1>	I/O + pulldown	47	TRG<2>	Out 3-State + pulldown
14	WIN<2>	I/O + pulldown	48	TRG<1>	Out 3-State + pulldown
15	WIN<3>	I/O + pulldown	49	TRG<0>	Out 3-State + pulldown
16	WIN<4>	I/O + pulldown	50	Vdd	Periphery AC
17	WIN<5>	I/O + pulldown	51	Vss	Periphery AC
18	WIN<6>	I/O + pulldown	52	AP<5>	I/O + pulldown
19	WIN<7>	In + pulldown	53	AP<4>	I/O + pulldown
20	WIN<8>	In + pulldown	54	AP<3>	I/O + pulldown
21	WIN<9>	In + pulldown	55	AP<2>	I/O + pulldown
22	FERDB	Out	56	AP<1>	I/O + pulldown
23	FEWRB	Out	57	AP<0>	I/O + pulldown
24	Vdd	Periphery AC	58	Vdd	Periphery AC
25	Vdd	Periphery DC	59	Vss	Periphery AC
26	nc		60	Vdd	Periphery DC
27	nc		61	Vdd	Core
28	Vdd	Core	62	Vdd	Periphery AC
29	Vdd	Periphery AC	63	Vdd	Periphery AC
30	Vdd	Periphery DC	64	Vss	Periphery AC
31	Vss	Core	65	PRGB	In Schmitt + pullup
32	SRST	In Schmitt + pullup	66	Vss	Periphery DC
33	HRST	In Schmitt + pullup	67	Vdd	Periphery DC
34	TCK	In + pulldown	68	PHI	In + pulldown

A3: BTI TQFP64 pinout

Pi n	Name	Type	Pin	Name	Type
1	Vdd	Core	35	Vdd	Core
2	Vdd	Periphery AC	36	Vss	Core
3	Vdd	Periphery AC	37	SRST	In Schmitt + pullup
4	Vss	Periphery AC	38	HRST	In Schmitt + pullup
5	PRG	In Schmitt + pullup	39	TCK	In + pulldown
6	Vss	Periphery DC	40	TMS	In Schmitt + pullup
7	Vdd	Periphery DC	41	TDI	In Schmitt + pullup
8	PHI	In + pulldown	42	TDO	Out 3-State + pullup
9	CK	In + pulldown	43	STRB	In Schmitt + pullup
10	Vss	Periphery DC	44	RWB	In Schmitt + pullup
11	Vdd	Periphery DC	45	HLB	Out 3-State + pulldown
12	SNPRST	In Schmitt + pullup	46	Vss	Periphery AC
13	Vdd	Periphery AC	47	Vss	Periphery AC
14	Vss	Core	48	Vss	Periphery DC
15	Vdd	Core	49	Vss	Core
16	Vss	Periphery DC	50	Vss	Periphery AC
17	nc		51	TRG<2>	Out 3-State + pulldown
18	Vss	Core	52	TRG<1>	Out 3-State + pulldown
19	Vss	Periphery AC	53	TRG<0>	Out 3-State + pulldown
20	WIN<1>	I/O + pulldown	54	Vdd	Periphery AC
21	WIN<2>	I/O + pulldown	55	Vss	Periphery AC
22	WIN<3>	I/O + pulldown	56	AP<5>	I/O + pulldown
23	WIN<4>	I/O + pulldown	57	AP<4>	I/O + pulldown
24	WIN<5>	I/O + pulldown	58	AP<3>	I/O + pulldown
25	WIN<6>	I/O + pulldown	59	AP<2>	I/O + pulldown
26	WIN<7>	In + pulldown	60	AP<1>	I/O + pulldown
27	WIN<8>	In + pulldown	61	AP<0>	I/O + pulldown
28	WIN<9>	In + pulldown	62	Vdd	Periphery AC
29	FERDB	Out	63	Vss	Periphery AC
30	FEWRB	Out	64	Vdd	Periphery DC
31	Vdd	Periphery AC			
32	Vdd	Periphery DC			
33	Vdd	Core			
34	Vdd	Periphery AC			

A4: Absolute maximum ratings

Parameter	Min	Max	Unit	Conditions
DC supply voltage	-0.5	4.1	V	
DC input diode current	-10	10	mA	
DC output diode current	-10	10	mA	
Time of outputs shorted		5	s	
Storage temperature	-65	150	°C	
Ambient free air temperature range	-40	85	°C	Industrial

A5: Recommended operating conditions

Electrical characteristics				
Parameter	Min	Typ	Max	Conditions
DC supply voltage	2.7V	3.3V	3.6V	
Low level input voltage	-0.5V		0.8V	2.7V to 3.6V TTL
"	-0.5V		0.3*Vdd	2.7V to 3.6V CMOS
High level input voltage	2V		Vdd+0.5V	2.7V to 3.6V TTL
"	0.7*VDD		Vdd+0.5V	2.7V to 3.6V CMOS
Low level output v.ge			Vss+0.1V	2.7V IOL=0.8mA CMOS
High level output v.ge	Vdd-0.1V			2.7V IOL=0.8mA CMOS
Low level output v.ge			0.4V	2.7V IOL=2 to 8 mA TTL
High level output v.ge	2.4V			2.7V IOL=2 to 8mA TTL
Pullups and pulldowns				
Pullup current	-66_A		-250_A	@0V worst case
Pulldown current	45_A		266_A	@3.3V worst case
AC output characteristics ²				
AP, TRG and HLB	0.021	0.033	0.056	ns/pF rise time
"	0.024	0.037	0.063	ns/pF fall time
WIN<6:1>	0.027	0.035	0.071	ns/pF rise time
"	0.030	0.040	0.081	ns/pF fall time
FEWRB and FERDB	0.030	0.040	0.081	ns/pF rise time
"	0.037	0.049	0.099	ns/pF fall time
AC input characteristics				
Input rise time			10ns	CMOS and TTL inputs
Input rise time			No limit	Schmitt inputs
Schmitt input threshold	1.39V	1.66V	1.8V	VT+
"	0.85V	1.05V	1.16V	VT-
Schmitt input hysteresis	0.48V	0.62V	0.66V	

¹ Worst case temperature, voltage and process corners.

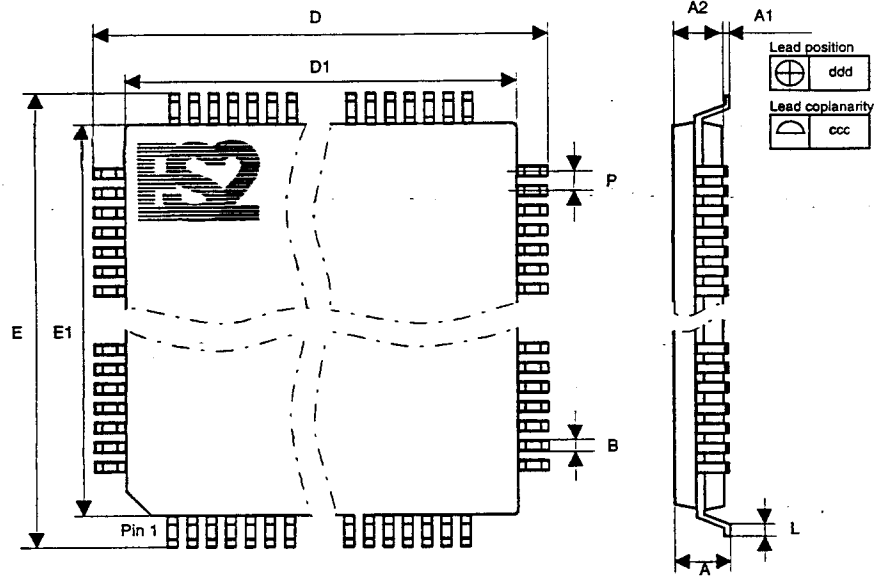
² Unless otherwise specified VDD=3.3V, T=25°C, typical process, rising/falling switching time=0.3ns.

A6: Package outlines



Package Selector Guide

(AG4-AO02/L)



**THIN PLASTIC QUAD FLAT PACK
BTQ xxx-001**

	BTQ044-001			BTQ064-001			BTQ080-001			BTQ100-001			BTQ144-001		
	44 LEAD	64 LEAD	80 LEAD	100 LEAD	144 LEAD										
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.40	1.50	1.60	1.40	1.50	1.60	1.40	1.50	1.60	1.40	1.50	1.60	1.40	1.50	1.60
A1	0.05	0.10	0.15	0.05	0.10	0.15	0.05	0.10	0.15	0.05	0.10	0.15	0.05	0.10	0.15
A2	1.35	1.40	1.45	1.35	1.40	1.45	1.35	1.40	1.45	1.35	1.40	1.45	1.35	1.40	1.45
D	11.90	12.00	12.10	11.90	12.00	12.10	15.90	16.00	16.10	15.90	16.00	16.10	19.90	20.00	20.10
D1	9.90	10.00	10.10	9.90	10.00	10.10	13.90	14.00	14.10	13.90	14.00	14.10	19.90	20.00	20.10
E	11.90	12.00	12.10	11.90	12.00	12.10	15.90	16.00	16.10	15.90	16.00	16.10	21.90	22.00	22.10
E1	9.90	10.00	10.10	9.90	10.00	10.10	13.90	14.00	14.10	13.90	14.00	14.10	19.90	20.00	20.10
L	0.45	0.60	0.75	0.45	0.60	0.75	0.45	0.60	0.75	0.45	0.60	0.75	0.45	0.60	0.75
P		0.80			0.50			0.65			0.50			0.50	
B	0.22	0.32	0.38	0.17	0.22	0.27	0.22	0.32	0.38	0.17	0.22	0.27	0.17	0.22	0.27
ccc		0.10			0.10			0.10			0.10			0.10	
ddd		0.10			0.10			0.10			0.10			0.10	

APPENDIX B: ANGLE AND POSITION EQUATIONS

B1: Angle equations

These equations give the track slope k that is function of the track angle with respect to the normal direction according to Eq.3. The quantities $\text{sum}(i,j)$ and $\text{dif}(i,j)$ are the sum and the difference respectively of shift times of wires i and j . The equations, giving integer unsigned values have an offset equal to the programmed ST value.

EqAB		TCEN	EqBC		TCEN
1L3L	$2*K0+\text{dif}(3,1)$	2	3L2R	$2*K0-\text{sum}(2,3)$	1
1R3L	$\text{sum}(1,3)$	0	3R2R	$\text{dif}(3,2)$	2
1R3R	$2*K0+\text{dif}(1,3)$	2	3L6L	$2*K0+\text{dif}(6,3)$	1
5L3L	$\text{dif}(3,5)$	2	3R6L	$\text{sum}(3,6)$	0
5L3R	$2*K0-\text{sum}(3,5)$	1	3R6R	$2*K0+\text{dif}(3,6)$	2
5R3R	$\text{dif}(5,3)$	2	7L6L	$\text{dif}(6,7)$	2
5R7L	$\text{sum}(5,7)$	0	7L6R	$2*K0-\text{sum}(6,7)$	1
			7R6R	$\text{dif}(7,6)$	2

Tab. B.1.1: AB and BC angle equation counters.

EqCD		TCEN	EqAC		TCEN
2R4L	$\text{sum}(2,4)$	0	1L2R	$2*K0-\text{sum}(1,2)/2$	4
2R4R	$2*K0+\text{dif}(2,4)$	2	1R2R	$K0+\text{dif}(1,2)/2$	5
6L8L	$2*K0-\text{dif}(6,8)$	2	1L6L	$2*K0-\text{dif}(1,6)/2$	5
6R8L	$\text{sum}(6,8)$	0	1R6L	$K0+\text{sum}(1,6)/2$	3
6R8R	$2*K0+\text{dif}(6,8)$	2	1R6R	$2*K0+\text{dif}(1,6)/2$	5
6L4L	$\text{dif}(4,6)$	2	5L2R	$K0-\text{sum}(2,5)/2$	4
6L4R	$2*K0-\text{sum}(4,6)$	1	5R2R	$\text{dif}(5,2)/2$	5
6R4R	$\text{dif}(6,4)$	2	5L6L	$K0-\text{dif}(5,6)/2$	5
9L7L	$\text{dif}(7,9)$	2	5R6L	$\text{sum}(5,6)/2$	3
9L7R	$2*K0-\text{sum}(7,9)$	1	5L6R	$2*K0-\text{sum}(5,6)/2$	4
			5R6R	$K0+\text{dif}(5,6)/2$	5
			9L6L	$\text{dif}(6,9)/2$	5
			9L6R	$K0-\text{sum}(6,9)/2$	4

Tab. B.1.2: CD and AC angle equation counters.

EqBD		TCEN	EqAD		TCEN
3L4R	$2*K0-\text{sum}(3,4)/2$	4	1L4L	$(4*K0-\text{dif}(1,4))/3$	8
3R4R	$K0+\text{dif}(3,4)/2$	5	1L4R	$2*K0-\text{sum}(1,4)/3$	7
3L4L	$K0-\text{dif}(3,4)/2$	5	1R4L	$(2*K0+\text{sum}(1,4))/3$	6
3R4L	$\text{sum}(3,4)/2$	3	1R4R	$(4*K0+\text{dif}(1,4))/3$	8
3R8L	$K0+\text{sum}(3,8)/2$	3	1R8L	$(4*K0+\text{sum}(1,8))/3$	6
3L8L	$2*K0-\text{dif}(3,8)/2$	5	5L4L	$(2*K0+\text{dif}(4,5))/3$	8
3R8R	$2*K0+\text{dif}(3,8)/2$	5	5R4L	$\text{sum}(4,5)/3$	6
7L4R	$K0-\text{sum}(4,7)/2$	4	5L4R	$(4*K0-\text{sum}(4,5))/3$	7
7L4L	$\text{dif}(4,7)/2$	5	5R4R	$(2*K0-\text{dif}(4,5))/3$	8
7R4R	$\text{dif}(7,4)/2$	5	5L8L	$(4*K0-\text{dif}(5,8))/3$	8
			5L8R	$2*K0-\text{sum}(5,8)/3$	7
			9L4R	$(2*K0-\text{sum}(4,9))/3$	7

Tab. B.1.3: BD and AD angle equation counters.

B2: Position equations

These equations give the track position x along the medium plane of the SL starting from the axis of wires 1 and 2 according to Eq.4.

EqBD		TCEN	EqAD		TCEN
3L2R	$(K0-\text{dif}(2,3))/2$	11	1L4L	$(\text{sum}(1,4)-K0)/2$	9
3L6L	$(K0+\text{sum}(3,6))/2$	9	1L4R	$(K0+\text{dif}(1,4))/2$	11
3R6L	$(3*K0-\text{dif}(3,6))/2$	11	1R4L	$(K0-\text{dif}(1,4))/2$	11
3R6R	$(5*K0-\text{sum}(3,6))/2$	10	1R4R	$(3*K0-\text{sum}(1,4))/2$	10
3R2R	$(3*K0-\text{sum}(2,3))/2$	10	1R8L	$(3*K0-\text{dif}(1,8))/2$	11
7L6L	$(3*K0+\text{sum}(6,7))/2$	9	5L4L	$(K0+\text{sum}(4,5))/2$	9
7L6R	$(5*K0-\text{dif}(6,7))/2$	11	5R4L	$(3*K0+\text{dif}(4,5))/2$	11
7R6R	$(7*K0-\text{sum}(6,7))/2$	10	5L4R	$(3*K0-\text{dif}(4,5))/2$	11
			5R4R	$(5*K0-\text{sum}(4,5))/2$	10
			5L8L	$(3*K0+\text{sum}(5,8))/2$	9
			5L8R	$(5*K0+\text{dif}(5,8))/2$	11
			9L4R	$(5*K0-\text{dif}(4,9))/2$	11

Tab. B.2.1: BC and AD position equation counters.

APPENDIX C: TRIGGER PATTERNS

Pattern	cAB	cBC	cCD	Type	x A	x B	x C	x D	Redundancies
1L3L2R4L	AC2	AC2	AC2				X		Redundant patt.
1L3L2R4R	AC1	ACL	AC1	1L1				R	1L3L2R_
1R3L2R4L	AC2	AC2	AC2					R	1R3L2R_
1R3L2R4R	AC2	AC2	AC2			X		R	1R3L2R_
1L3L6L4R	AC1	AC1	ACL	11L				X	
1R3L6L4R	AC2	AC2	AC2						
1R3R6L4R	AC2	AC2	AC2				X		
1R3R6L8L	AC1	ACH	AC1	1H1					
1R3R6R8L	AC1	AC1	ACH	11H				X	
1R3L6L8L	ACH	AC1	AC1	H11	X				
5L3L2R4L	AC2	AC2	AC2				X		
5L3R2R4L	AC2	AC2	AC2						
5R3R2R4L	AC1	AC1	ACH	11H					
5L3R6L4L	AC2	AC2	AC2			X			
5L3R6L4R	AC2	AC2	AC2						
5R3R6L4L	AC1	ACH	AC1	1H1					
5R3R6L4R	AC2	AC2	AC2				X		
5L3R6L8L	AC2	AC2	AC2			X			
5L3R6R8L	AC2	AC2	AC2						
5L3R6R8R	ACL	AC1	AC1	L11	X	R			5L_6R8R
5R7L6L4R	AC2	AC2	AC2						
5R7L6R4R	AC2	AC2	AC2			X			
5R7L6L4L	ACH	AC1	AC1	H11	X				
9L7L6L4R	AC1	AC1	ACL	11L				X	
9L7L6R4R	AC1	ACL	AC1	1L1				R	9L7L6R_
9L7R6R4R	ACL	AC1	AC1	L11	X			R	9L7R6R_
5L7L6R8L	AC2	AC2	AC2		R		X		_7L6R8L
5L7L6R8R	AC1	ACL	AC1	1L1					Redundant patt.
5R7L6R8L	AC2	AC2	AC2						Redundant patt.
5R7L6R8R	AC2	AC2	AC2						Redundant patt.
9L7L6R8L	AC2	AC2	AC2						Redundant patt.
9L7R6R8L	AC2	AC2	AC2						Redundant patt.

Tab. C.1: The BTI recognizable track patterns.

Recognizable tracks are classified into patterns. Patterns are partially or totally masked in order to minimize redundancies between adjacent BTIs. cAB, cBC and cCD are the alignment acceptances respectively for EqAB, EqBC and EqCD with respect to EqAD. The four possible

acceptances are specified by the programmable parameters AC1, AC2, ACH and ACL as specified in section 7.3.

$\bar{x}A$, $\bar{x}B$, $\bar{x}C$ and $\bar{x}D$ are the low quality trigger mask respectively for a wrong or missing A plane, B, C and D. The low quality triggers are normally enabled with two exceptions: X-type patterns (marked with X) and redundant patterns (marked with R). These two classes of low quality triggers are enabled setting high the correspondent flag XON and RON. High quality redundant patterns are enabled setting high RON.

APPENDIX D: DRIFT VELOCITY CODING

4ST3	4RE3	DEAD	Latency (ns)	ST	V_d ($\mu\text{m}/\text{ns}$)
32	0	23	400	24	70.0
32	2			24.5	68.6
33	1	24	425	25	67.2
34	0			25.5	65.9
34	2	25	425	26	64.6
35	1			26.5	63.4
36	0	26	450	27	62.2
36	2			27.5	61.1
37	1	27	450	28	60.0
38	0			28.5	58.9
38	2	28	475	29	57.9
39	1			29.5	56.9
40	0	29	475	30	56.0
40	2			30.5	55.1
41	1	30	500	31	54.2
42	0			31.5	53.3
42	2	31	500	32	52.5
43	1			32.5	51.7
44	0	32	525	33	50.9
44	2			33.5	50.1
45	1	33	525	34	49.4
46	0			34.5	48.7
46	2	34	550	35	48.0
47	1			35.5	47.3
48	0	35	550	36	46.7

Tab. D.1: 4ST3, 4RE3, DEAD parameters and expected trigger latency for different drift velocities. ST values correspondent to 4ST3 and 4RE3 parameters. 2ST, 3ST, 4ST, 5ST and 7ST are equal to ST multiplied by 2, 3, 4, 5 and 7 respectively. The ST value is given in units of 12.5ns and the apparent drift velocity V_d is computed for a maximum drift length of 2.1cm.

APPENDIX E: CHIP VALIDATION USING BIST CIRCUIT.

Chip validation is simplified if internal built-in self test circuitry is used. This block allows to exert all track patterns at high speed with a programmed track angle and position. The test sequence consists of the following steps:

E1: Initial configuration file setup and validation test start

The BTI Config register file is programmed for chip validation: all wire enable masks are set high (WEN=11111111), wire dead time is the maximum possible (DEAD=111111), all trigger angle windows are set to the limits (high=111111 low=000000) and any combination of ACx is accepted.

The BTI Test register file is programmed for validation: all pattern masks are set high (PTMSK=\$FFFFFFFF), all equation counter group masks are disabled (TCEN=\$000). As described in Appendix B equation counters are grouped into 12 ensembles with an individual counter enable bit in TCEN. Test sequence starts pulling low SYRSB, setting high RON, XON and TEST, equation counters are all enabled setting high the group mask (TCEN=\$FFF). When SYRSB is released the test starts at the first rising clock edge.

E2: Equation counters settings

TCEN GROUP	Step	TCEN GROUP	Step
0	2	6	2/3
1	2	7	2/3
2	2	8	2/3
3	1	9	1
4	1	10	1
5	1	11	1

Tab. E.2.1: Equation counters step/cycle.

Group	15cy	+2cy	+14cy	+2cy	+14c y	+2cy	+13c y
0	1	0	0	0	0	0	0
1	1	1	0	0	0	0	0
2	1	0	0	0	0	0	0
3	1	1	1	0	0	0	0
4	1	1	1	1	0	0	0
5	1	1	1	0	0	0	0
6	1	1	1	1	1	0	0
7	1	1	1	1	1	1	0
8	1	1	1	1	1	0	0
9	1	1	1	0	0	0	0
10	1	1	1	1	0	0	0
11	1	1	1	1	1	1	1

Tab. E.2.2: TCEN sequence used to preset all equations to \$1F.

All equations count starting from zero with a counting step to clock rate dependent on group: In order to scan all track patterns it is necessary to preset all equation counters to the same value. This is achieved during the counting sequence, disabling each group as soon as it has the right output value. For example to reach the common value \$1F equation counter groups are enable for the number of cycles given in the following table: The group 0 and 2 are stopped (TCEN(0)=0) after 15 clock cycles, group 1 is stopped 2 cycles later, group 3, 5 and 9 are stopped 14 cycles later. At the 62th cycle when group 11 is stopped all equation counters have the same value (\$1F in this case).

E3: Track patterns sequencing

When all equation counters are preset to the same value track patterns can be enabled one by one using the validation sequencer. The execution starts setting high the VALTST flag. Each pattern is tested for an equation coincidence in different conditions as given in table E.3.1

Each trigger pattern needs 13 clock cycles to try all the test conditions, this means that track patterns are all tested with 832 cycles. Of course to reach a good fault coverage the validation sequence must be repeated for at least two different equation counters values and with different drift velocity parameters. The validation sequence repeated for angle values \$1F and \$20 gives a net toggling coverage around 92%.

Seq. cycle	XON	RON	XA	XB	XC	XD	Conditions
1	1	1	1	0	0	0	Rid. on, Xeq on, Low -A
2	1	0	1	0	0	0	Rid. off, Xeq on, Low -A
3	0	0	1	0	0	0	Rid. off, Xeq off, Low -A
4	1	1	0	1	0	0	Rid. on, Xeq on, Low -B
5	1	0	0	1	0	0	Rid. off, Xeq on, Low -B
6	0	0	0	1	0	0	Rid. off, Xeq off, Low -B
7	1	1	0	0	1	0	Rid. on, Xeq on, Low -C
8	1	0	0	0	1	0	Rid. off, Xeq on, Low -C
9	0	0	0	0	1	0	Rid. off, Xeq off, Low -C
10	1	1	0	0	0	1	Rid. on, Xeq on, Low -D
11	1	0	0	0	0	1	Rid. off, Xeq on, Low -D
12	0	0	0	0	0	1	Rid. off, Xeq off, Low -D
13	1	1	1	1	1	1	Rid. on, Xeq on, High

Tab. E.3.1: Track pattern test sequence of conditions.