**CMS - PADOVA**

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**DRAFT**

# Track Correlator

# User manual

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## 1. Introduction

The proposed baseline of the DTBX chamber trigger is a multistage scheme.

The front-end trigger device is called Bunch and Track Identifier (BTI)[1]: it performs a rough track reconstruction and uniquely identifies the parent bunch crossing of the candidate track by means of a generalized mean-timer technique. First prototypes were already produced.

The BTI is followed in the electronics chain by a Track Correlator (TRACO) that is required to associate portions of tracks in the same chamber relating predefined groups of BTIs among them.

A third device, called Trigger Server[2], performs the track selection within a full chamber and forwards information to the Muon Regional Trigger[3], that finally extracts the track candidate transverse momentum.

## 2. Short Description of BTI

The Bunch and Track Identifier was studied to work on each groups of four layers of staggered drift tubes called Super Layers (SL), aiming to the identification of the tracks giving a signal in at least three of the planes. We quickly recall the basic description of the device: any other detail can be found in Reference 4.

Each BTI is connected to nine wires allocated as shown in Figure 1.

The parameters computed from the BTI are the angular k-parameter $k = h \tan \psi$ (the track direction) and the crossing position, computed in the SL central plane. The geometrical quantities involved are shown in Figure 1: $\psi$ is the angle of the track with respect to the normal to the chamber and $h = 1.3mm$ is the distance between the wire planes.

These parameters are evaluated by means of a generalized mean-timer technique: this method is a search inside a BTI for the alignments of the recorded hits belonging to a track. If there is an alignment of four hits the signal is marked as High Quality Trigger (HTRG), while if it is due to the alignment of only three hits, it is marked as Low Quality

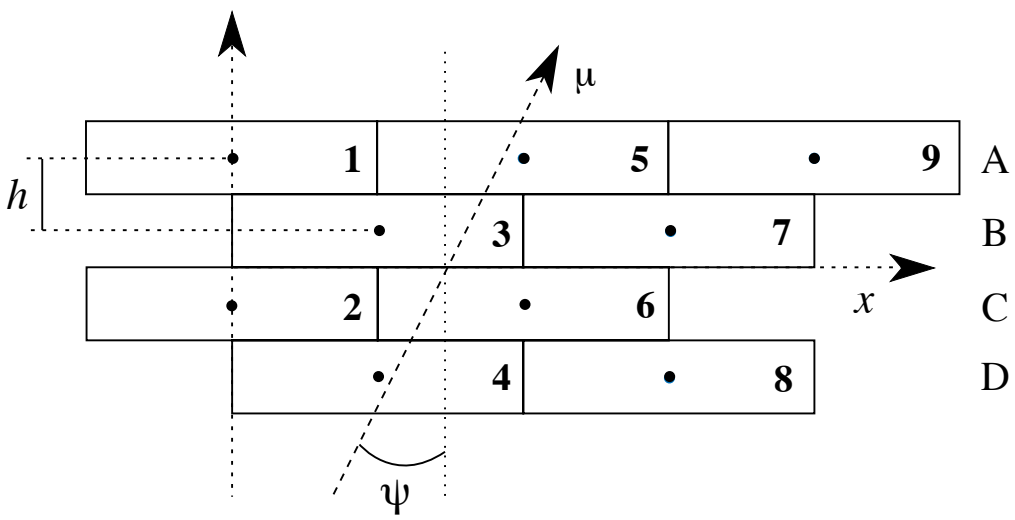



Figure 1 - BTI layout showing channels allocation.

Trigger (LTRG).

The alignment occurs with fixed delay with respect to the parent bunch crossing time, thus permitting its identification. The total latency of the BTI is determined by the maximum drift-time to the wires, $T_{MAX}$, plus 4 clock cycles needed for input signal synchronization and BTI calculations. For a nominal drift velocity of 50 μm/ns the delay of the TRG signal with respect to the parent interaction is therefore 20 bunch crossings.

The BTI trigger algorithm actually generates HTRGs and LTRGs when the computed k-parameters of any of the predefined patterns of wires are equal within the programmed tolerance. The definition and the full list of the preloaded patterns is available in Reference 4.

Position and angular resolution of the device depend on the drift velocity and on the sampling frequency of the device. For a nominal drift velocity of 50 μm/ns and a sampling frequency of 40 MHz, the angle is measured with a resolution better than 60mrad, while the position is measured with a resolution of 1.25mm. The angular resolution is track pattern dependent and is generally worse for LTRGs.

Using the current geometric parameters of the chamber, as described in version 113 of the CMS detector sofware, the angular acceptance is nominally $\psi_{MAX} = \pm 55°$.

Each SL is equipped with one BTI every four wires and the BTIs are overlapped by five wires assuring that every track, with angle within the maximum acceptance range, is fully contained in at least one BTI.

K-parameter and position of the track as measured from the corresponding equations, coded in 6 bits, and one trigger quality bit, marking HTRG or LTRG (H/L), are transmitted to the TRACO on the BTI track-data bus.

Only one track per bunch crossing per BTI is forwarded to the TRACO.

## 3. Track Correlator layout

The DTBX chamber is composed of two SL in the CMS transverse plane (φ view) and one SL in the longitudinal one (θ view). Each SL is equipped with BTIs.

The TRACO is a processor that interconnects the two SL of the transverse plane. It receives the information from the BTI devices connected to it and tries to find the couple of BTI track segments that fits the best track, linking the inner layer candidates to the

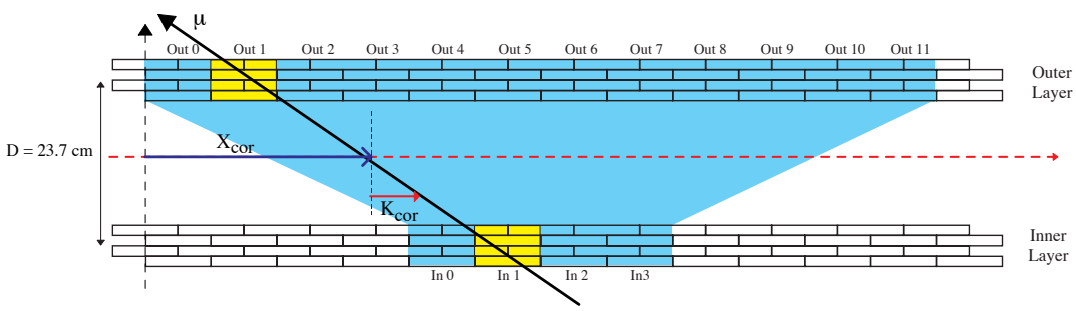



Figure 2 - Track Correlator layout

outer layer ones.

The number of BTIs connected to a TRACO is limited from the size of the chip and it is determined by the acceptance requirement. The final design connects four BTIs of the inner Superlayer to twelve BTIs of the outer Superlayer allocated as shown in Figure 2.

The introduction of this device is necessary since the BTI is intrinsically a noisy device and therefore a local preselection and a quality certification of the BTI triggers is required. Furthermore the number of BTIs per chamber is around few hundreds and it is not possible to connect together all the channels to perform any preselection at chamber level.

## 4. Track Correlator Specifications

The block diagram of the TRACO operations is given in Figure 3. In the following paragraphs we shall describe the TRACO algorithm referring to the flow of this diagram.

### 4.1 Data paths

In order to allow the identification of two muons inside the same correlator, the TRACO algorithm is applied twice to the data received from the BTI. Therefore inside the TRACO there are two parallel flows delayed by one cycle: the first path computes a First Track, choosing between all the BTI candidates, while the delayed path computes a Second Track from all unused candidates. The programmability of the preferences for the choice of the First Track and the Second Track are completely independent, although in principle we believe that the same criteria should apply.

Inside the full system a further selection is needed in the case that more than one TRACO inside a chamber give a trigger. The communication between the TRACOs and the chamber trigger server to allow this decision is done using a dedicated PREVIEW data bus for each track, in order to minimize the time needed for calculations of the whole trigger chain. A copy of the converted angle (see paragraph 4.3) of one of the candidates chosen for correlation is sent to the Trigger Server according to the programmed H/L and IN/OUT selection flags, as soon as the correlation calculation has been performed. The Trigger Server selection is based on the quality of the PREVIEW of the various candidates. The preview data is composed by 9 bits: five bits for the module of the converted angle, one bit for the track quality (H/L); one bit identifying First/Second track; one bit identifying Inner/Outer layer; one bit identifying Correlated/Uncorrelated track candidate.

### 4.2 Input Register (16 x 8bits)

This register receives and latches the data values and the qualification flags from the BTI chip. The TRACO collects the inputs from 16 BTIs (four from the inner layer and twelve from the outer layer).

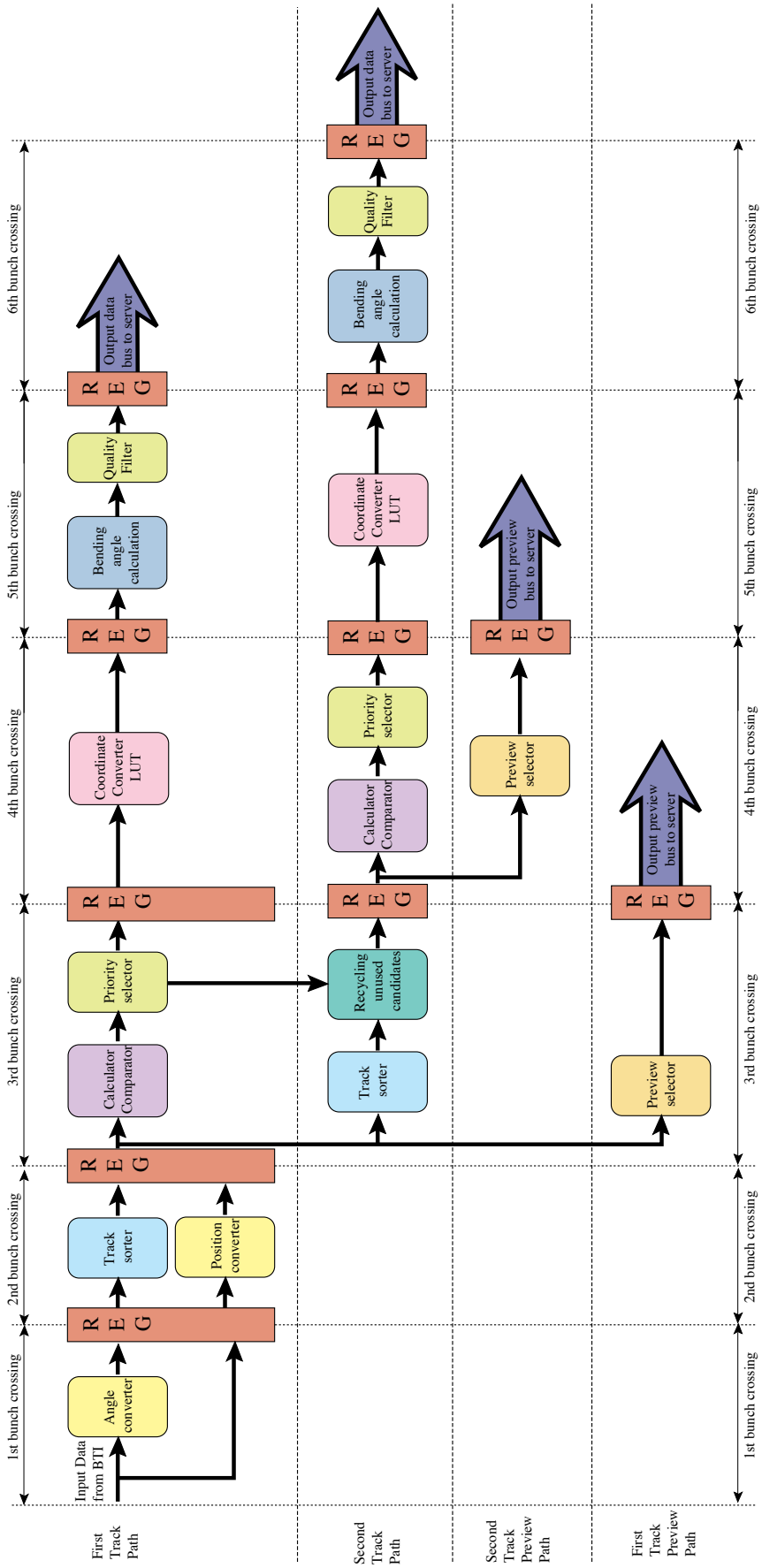



Figure 3 - TRACO Block Diagram

From each BTI the input data bus contains the k-parameter and the position in the BTI coordinate system, multiplexed at 80MHz on the same lines (6 bits wide). Two extra flags are provided: the trigger quality (H/L) and the strobe. TRACO inputs latch the k-parameter on the rising edge of clock and the position on the next falling edge. (timing ?)

### 4.3 Angle and position converter

This module receives the k-parameter 6 bits input word from the BTI and converts it into local radial coordinates

$$k_{local} = k_{BTI} - RAD - BTIC$$

The RAD parameter is a 5 bits programmable value, depending on the geographical position of the correlator, i.e. the k-parameter of radial tracks passing through its center. The BTIC is a 6 bits programmable value dependent on the maximum drift time the BTI is programmed for: BTI k parameter has an offset equal to the programmed maximum drift time (ST parameter); meaning that orthogonal tracks have k value equal to ST. The converted angle is used for internal calculations and sent on the Preview bus to the Trigger Server for further track selection.

Each BTI position is converted to TRACO position, offsetting by the appropriate geographical value. An additional Superlayer shift parameter is provided to correct for eventual construction misalignments of the two quadruplets: a programmable 6 bits value IBTIOFF is added to inner positions.

### 4.4 Sorter

This module receives the converted angle and selects the candidate with the smallest angle,i.e. the angle closest to the local radial direction. There are two sorters for the four inner BTIs and two for the twelve outer BTIs, in order to select the two best candidates for the first track and for the second track in pipeline. The choice is done twice independently on the two φ Superlayers.

The sorting operation can be programmed to select the biggest angle (FHISM and SHISM) instead of the smallest one, and/or to give preference to candidates tagged with the HTRG quality flag (FHTPRF and SHTPRF).

### 4.5 Calculator and Comparator

This module computes the k-parameter and the position of the correlated candidate. It transforms the inner and outer k-parameter of the two independently selected track segments into the correlator coordinates system and computes the correlated track parameters.

The internal parameters computed for the correlated tracks are:

$$\begin{cases} k_{COR} = \dfrac{D}{2}\tan\psi = x_{inner} - x_{outer} \\ x_{COR} = \dfrac{\left(x_{inner} + x_{outer}\right)}{2} \end{cases}$$

where D is a 5 bits value representing the ratio of the distance between the two Superlayers and the distance of two wire planes in a Superlayer. Only three values are allowed: 16, 18 and 20. The angular resolution of a correlated track candidate is 10mrad for the nominal drift velocity, thus improving the BTI value by almost an order of magnitude, while the resolution on the position is unchanged.

A second step compares the k-parameter of inner track, outer track and correlated calculation. If the correlated value fits inside the programmed acceptance window (FPRGCOMP<1:0> and SPRGCOMP<1:0> for first and second track candidates respectively) with respect to the parent segments the correlation flag is raised. The acceptance window can be set either to 0, asking for equality in the comparison, or to 1,2 and 3 corresponding to 1,2 and 3 bit of difference.

### 4.6 Priority Selector and Preview Selector

This module selects one of the candidates according to some programmed information.

If the correlation was successful the priority selector chooses the correlated candidate and forwards its parameters to the further stages.

If the correlation fails the correlator creates an uncorrelated track following a preference list that includes the parent superlayer (Inner or Outer) and the quality bit (High or Low) of the two candidate tracks.

If no correlation is possible since there is no candidate in one Superlayer, the existing uncorrelated track is still accepted.

A preference selection can be activated to connect the trigger generated in the transverse view to the triggers generated from the BTIs in the longitudinal view. A programmable coincidence between the two views is foreseen to certify the uncorrelated triggers. In particular, since the noise generated from the BTI algorithm is concentrated in the LTRGs, this coincidence is requested by default for the LTRGs and it is optional for the HTRGs.

The First and the Second Track priority selectors treat the *best* inner candidate, the *best* outer candidate and the correlated candidate considering the trigger quality, the high level trigger mask (HTMSK), the low level trigger mask (LTMSK) and the Superlayer mask (SLMSK). The meaning of selection bits is given in the Table 1.

| | |
|---|---|
| F(S)HTMSK | Single High quality triggers:<br>(1) accepted only if coincident with Theta trigger<br>(0) always accepted (default) |
| F(S)LTMSK | Single Low quality triggers:<br>(1) always discarded<br>(0) accepted only if coincident with Theta trigger (default) |
| F(S)SLMSK | Superlayer preference:<br>(1) outer<br>(0) inner |

Table 1 – Track selection configuration bits.

Each priority selector sends only one candidate towards the output bus, and generates a three bits qualification code as shown in Table 2.

| ***Description*** | ***Symbol*** | ***Code*** |
|---|---|---|
| HTRG on inner and outer layer (correlated) | HH | 0 |
| HTRG on inner/outer layer and<br>LTRG on outer/inner layer (correlated) | HL | 1 |
| LTRG on inner and outer layer (correlated) | LL | 2 |
| HTRG on outer layer | $H_o$ | 3 |
| HTRG on inner layer | $H_i$ | 4 |
| LTRG on outer layer | $L_o$ | 5 |
| LTRG on inner layer | $L_i$ | 6 |
| Null track | | 7 |

Table 2 - Codes for output track quality identifier.

### 4.7 Recycling unused candidates

Two candidates are needed to fit a correlated track, one from the inner Superlayer and another from the outer one. If the correlated track does not satisfy the programmed acceptance value, only one of the track candidates selected to try the correlation is forwarded as the First Track choice. The other candidate must be reused for the Second Track calculations. This module allows either to enable or to disable this recycling task according to two programming bits: REUSEI and REUSEO with the meaning shown in Table 3.

| | |
|---|---|
| REUSEI | Inner candidate:<br>(1) recycling enabled<br>(0) no recycling |
| REUSEO | Outer candidate:<br>(2) recycling enabled<br>(0) no recycling |

Table 3 – Recycling configuration bits.

### 4.8 Mixer

The two selected tracks are output on the same bus at consecutive bunch crossings. Therefore it is possible that a Second Track from the previous bunch crossing is computed at the same time of a First Track from the bunch crossing being considered. A First Track choice has always priority on the output bus and therefore any First Track

overlaps the Second Track choice from the previous bunch crossing. A flag is activated if an overlap occurs.

### 4.9 Coordinate converter and bending angle calculation

The internally calculated position and k-parameter are converted, to the chamber reference system: position is transformed to radial angle $\phi$ and k-parameter to bending angle $\phi_b$ as defined in Figure 4.

This task is performed passing track candidates k-parameter and position through two programmable look-up tables. The first look-up table is used for conversion of the position, coded in 9 bits, to the track radial angle $\phi$, coded in 12 bits (11 bits plus the sign with 12 bits resolution). The second table performs the conversion from the k-parameter, coded in 10 bits to the angle with respect to the normal to the chamber $\psi$, coded in 10 bits (9 bits plus the sign with 9 bits resolution).

A further block performs the computation of the bending angle:

$$\phi_b = \phi - \psi$$

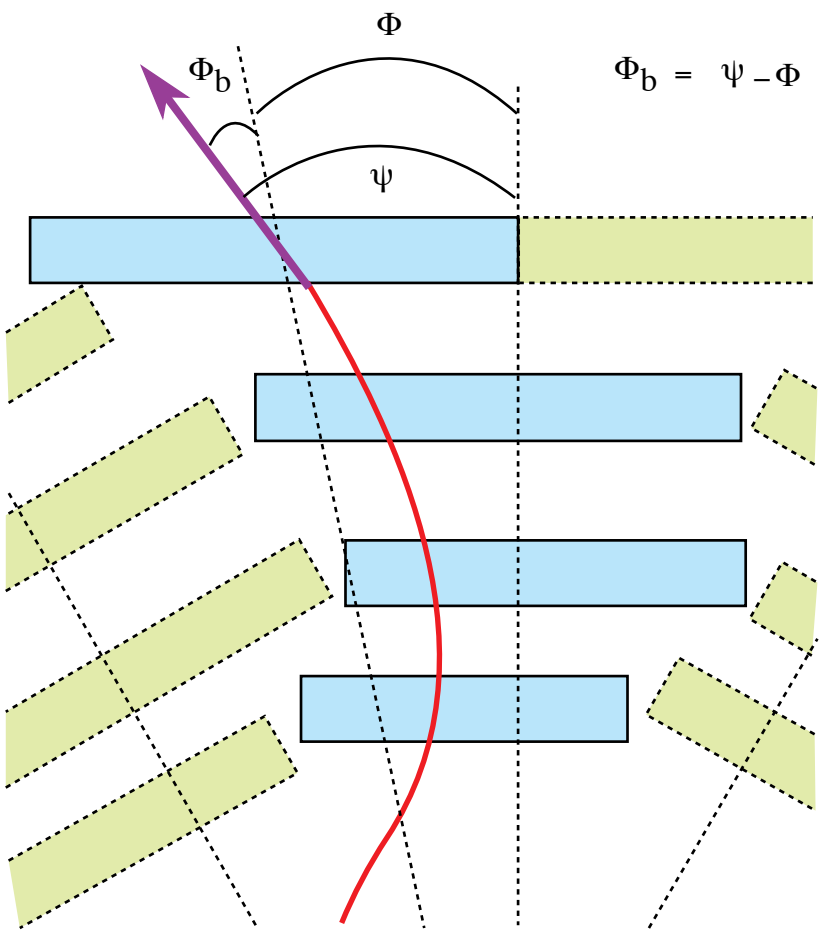



Figure 4 - Definition of the TRACO output parameters.

### 4.10 Quality filter

Some filtering functions are performed in this block to select the output value driven to the chamber server. These functions include the suppression of single low quality triggers (LTS) and a programmable acceptance window for the bending angle output value. With the LTS filter activated, double correlated and single low quality triggers are cancelled when they come within 4 clock cycles before a high quality trigger. The angular cut is applied to low quality triggers, either double correlated or single; when the absolute value of the bending angle is higher than a programmed value (KPRGCOM) the trigger is cancelled. The filters will be discussed in detail in paragraph 5.3.

### 4.11 Output Preview-Data Bus

TRACO Preview-Data bus provides one track at each clock cycle, with up to two tracks per bunch crossing at consecutive clock cycles.

The latency for the first track is three cycles, while the second one is output in the next cycle. In case two events generate triggers in two consecutive crossings and two tracks are detected correspondent to the first event, the second track of the first event is suppressed to allow the first track of the next event to be forwarded.

Selected tracks are output on a 9 bits bus, where 5 bits give the absolute value of the k-parameter, 1 bit the sign, and 3 bits the trigger quality: Correlated (SRVPCR), High/Low (SRVPHL) and Inner/Outer (SRVPIO). One bit is the first track strobe. The Preview bus is described in Table 4.

| | |
|---|---|
| SRVPR<4:0> | Track k-parameter<br>$1F is the default value for no trigger |
| SRVPR<5> | Sign of track k-parameter |
| SRVPCR | Flag for correlated track |
| SRVPHL | Flag for high/low (1/0) quality track |
| SRVPIO | Flag for Inner/Outer track<br>(1) Outer trigger<br>(0) Inner trigger |
| SRVPFS | Strobe for first track output<br>(1) First track<br>(0) Second track (if SRVPR <> $1F) or no trigger |

Table 4 – TRACO Preview-Data bus.

### 4.12 Output Trigger Data Bus

TRACO Data Bus provides one track at each clock cycle, with up to two tracks per event at consecutive clock cycles.

The latency for the First Track is five cycles, while Second Tracks are output one cycle later. Similarly to the Preview-Data bus in case there are two events at contiguous bunch

crossings, the second track from the first event is suppressed and the first track from the second event is forwarded.

The selected track is output on a bus, using 10 bits for the bending angle, 12 bits for the radial angle and three quality bits identifying track quality. One bit is the first track strobe. The Preview bus is described in Table 5.

| | |
|---|---|
| SRVDT<26:15> | Radial angle (signed integer) |
| SRVDT<14:5> | Bending angle (signed integer) |
| SRVDT(4:2) | Track quality |
| SRVDT(1) | Overlap flag<br>(1) track overlap |
| SRVDT(0) | Strobe for first track output<br>(1) First track<br>(0) Second track (if SRVPR <> $1F) or no trigger |

Table 5 – TRACO Data bus.

## 5. TRACO Interfaces

The following paragraphs describe TRACO interfaces for control and monitoring.

### 5.1 Control Logic

This block contains a JTAG[1] interface and a bi-directional parallel interface. The JTAG port (tms, tck, tdi, tdo) can be used either to verify chip interconnections once it has been mounted on a PCB or to program internal registers. An additional capability of this interface is the monitoring of chip activity without interfering with the trigger function. This can be performed simply reading the snap registers connected to the input signals and to the output bus (see snap registers description in the next paragraph).

While both the parallel interface and the JTAG bus can be used to program the TRACO internal registers, only the parallel interface, much faster than the JTAG port, can be used to load the look-up tables needed for coordinate conversion. Using the dedicated preview bus the TSS has the possibility to access the internal registers of the connected TRACOs and downstream the Trigger Server Master (TSM) can access all chamber TSS.

### 5.2 Reset Logic

At power on all trigger chips can be put in a default state using the asynchronous reset line HRSTB. The synchronous reset (SYRSB) can be used to clear all internal registers with the exception of the configuration parameter register file.

An additional synchronous reset command (SNRSB) clears only the snap registers.

[1] IEEE Std 1149.1-1990 "IEEE Standard Access Port and Boundary-Scan Architecture", May 21, 1990

### 5.3 Internal register files

TRACO registers are grouped into 5 files of 8 bit words accessible using dedicated JTAG instruction addresses: configuration, test, snap, debug and boundary.

The CONFIG register file (Tab 5.3.1) collects all the set up registers for TRACO trigger operation and has to be programmed after a power-on reset (HRSTB low).

The section 7.0: Operating Instructions gives more information about the use of these parameters. The TEST register file (Tab. 5.3.3) is mainly used to run self-tests of the TRACO. The section 8.0: Test and Debug Features gives more information about track emulation procedure. The SNAP register file (Tab. 5.3.4) is used for chip monitoring purposes. The snap registers are cleared by a SNPRST signal and are written only once, after the first trigger occurrence. The DEBUG register must be used only to debug and verify chip prototypes. The Boundary Scan register (see Tab. 5.3.5) is accessible via JTAG and is used only for Trigger board connectivity tests.

The Configuration register file is described in Table 5.3.1.

BTIC<5:0> is the offset of BTI k-parameter: when the latched k-parameter is equal to BTIC the track angle is supposed to be orthogonal to the chamber.

RAD<4:0> is the k-parameter correspondent to a radial track. (?)

DD<4:0> must be set equal to the ratio between the distance of Superlayer median planes in the chamber and distance of wire planes in the Superlayer. The allowed values are 16, 18 and 20.

F/SPRGCOMP<1:0> are used to set the alignment tolerance of track segments for correlated tracks. Two track segments generate a correlated track when the k-parameters of the candidates and the k-parameter of the correlated track (calculated from segment positions) are equal within a given tolerance. This tolerance can be programmed from 0 to 3. FPRGCOMP is the alignment tolerance for first track calculation while SPRGCOMP is for the second.

| Add | MSB-LSB |
|---|---|
| 0 | RAD<1:0>, BTIC<5:0> |
| 1 | DD<4:0>, RAD<4:2> |
| 2 | REUSEI, FHTMSK, FLTMSK, FSLMSK, FHTPRF, FHISM, FPRGCOMP<1:0> |
| 3 | REUSEO, SHTMSK, SLTMSK, SSLMSK, SHTPRF, SHISM, SPRGCOMP<1:0> |
| 4 | SNAPCOR<2:0>, PRGDEL<2:0>, LTS, LTF |
| 5 | TRGENB<8:1> |
| 6 | TRGENB<16:9> |
| 7 | IBTIOFF<5:0>, TRGADEL<1:0> |
| 8 | KPRGCOM<7:0> |
| 9 | PRVSIGNMUX, STARTTEST, TESTMODE |

Setting high F/SHISM makes the track candidate sorter to look for higher bending angles instead of lower (default).

Setting high F/SHTPRF makes the candidate sorter to look for the best candidate considering high quality tracks only.

Setting high F/SSLMSK makes the sorter to prefer outer candidates when trigger quality is the same. The default value is 0 considering that the outer triggers can be generated twice because of overlap between neighbouring TRACOs.

Setting high F/SLTMSK makes to discard all low quality trigger candidates. The default value is 0 allowing to consider them only if there is a coincidence with a trigger from the theta Superlayer (THETA input).

Setting high F/SHTMSK makes all high quality trigger candidates to be considered only if there is a coincidence with a trigger from the theta Superlayer (THETA input). The default value is 0 making them to be always considered.

If REUSEI and REUSEO are set high the unused candidates selected for the first track choice (for example from a failed correlation the inner candidate is selected and the outer one is discarded) can be used for the second track choice.

LTF is in logic OR with THETA input. If LTF is set high the only way to discard low quality trigger candidates in the sorting algorithm is to set the F/SLTMSK bit.

If LTS is set high the low trigger suppression algorithm is turned on. All low quality triggers, either single or correlated, are cut when followed within 4 clock cycles by any high quality trigger. This LTS algorithm is a complement to the LTS algorithm implemented in the BTI where low quality triggers, time-correlated with a high quality one, can be suppressed in the range –1 to +8 clock cycles.

PRGDEL is a programmable delay for trigger data output. The latency of trigger data bus (SRVDT) can be increased by a maximum of 7 clock cycles. When PRGDEL is equal

| SNAPCOR | Output snap register selection |
|---|---|
| 000 | Any |
| 001 | Any Inner |
| 010 | Any Outer |
| 011 | Any Inner AND Outer |
| 100 | Any High quality |
| 101 | Inner High quality |
| 110 | Outer High quality |
| 111 | Inner AND Outer High quality |

to 0 the latency of SRVDT is the lowest and is equal to 5/6 clock cycles for the first/second track candidate.

| Address | MSB-LSB |
|---|---|
| 10 | ANG1<1:0>, POS1<5:0> |
| 11 | POS2<1:0>, TRG1, HLB1, ANG1<5:2> |
| 12 | ANG2<3:0>, POS2<5:2> |
| 13 | POS3<3:0>, TRG2, HLB2, ANG2<5:4> |
| 14 | ANG3<5:0>, POS3<5:4> |
| 15 | POS4<5:0>, TRG3, HLB3 |
| 16 | TRG4, HLB4, ANG4<5:0> |
| 17 | ANG5<1:0>, POS5<5:0> |
| 18 | POS6<1:0>, TRG5, HLB5, ANG5<5:2> |
| 19 | ANG6<3:0>, POS6<5:2> |
| 20 | POS7<3:0>, TRG6, HLB6, ANG6<5:4> |
| 21 | ANG7<5:0>, POS7<5:4> |
| 22 | POS8<5:0>, TRG7, HLB7 |
| 23 | TRG8, HLB8, ANG8<5:0> |
| 24 | ANG9<1:0>, POS9<5:0> |
| 25 | POS10<1:0>, TRG9, HLB9, ANG9<5:2> |
| 26 | ANG10<3:0>, POS10<5:2> |
| 27 | POS11<3:0>, TRG10, HLB10, ANG10<5:4> |
| 28 | ANG11<5:0>, POS11<5:4> |
| 29 | POS12<5:0>, TRG11, HLB11 |
| 30 | TRG12, HLB12, ANG12<5:0> |
| 31 | ANG13<1:0>, POS13<5:0> |
| 32 | POS14<1:0>, TRG13, HLB13, ANG13<5:2> |
| 33 | ANG14<3:0>, POS14<5:2> |
| 34 | POS15<3:0>, TRG14, HLB14, ANG14<5:4> |
| 35 | ANG15<5:0>, POS15<5:4> |
| 36 | POS16<5:0>, TRG15, HLB15 |
| 37 | TRG16, HLB16, ANG16<5:0> |

Tab 5.3.3: TEST register file.

SNAPCOR can be used to choose the kind of trigger will be stored in the output snap registers. The programming possibilities are described in Table 5.3.2.

TRGENB are the mask bits for BTI inputs. Setting high any bit in this register makes the correspondent BTI input to be disabled.

TRGADEL is a programmable delay for the THETA trigger input. From 0 to 3 clock cycles can be added to this trigger input in order to synchronise with the internal operation. The THETA trigger is expected to arrive at the TRACO input pin two clock cycles after the reception of a trigger from the BTI inputs.

IBTIOFF is an offset value added to any track position for the Inner Superlayer. A misalignment of the two Superlayers can be corrected programming this register accordingly. All position values for the Inner BTIs are corrected adding the IBTIOFF programmed value before performing any calculation.

KPRGCOM is the parameter setting the angular cut for single and correlated low quality triggers. All low quality triggers are cut when half the absolute value of the bending angle is higher than KPRGCOM.

TESTMODE and STARTTEST are respectively the enable flag and the start bit for track emulator circuitry. When TESTMODE is set to 1 all BTI inputs are disabled and the track emulation logic is enabled; the TEST register file is programmed to produce a given track pattern. The emulation starts when the STARTTEST bit is set to 1.

PRVSIGNMUX has to be set to 0 for normal operation. If PRVSIGNMUX is set to 1 the meaning of part of the output bus (SRVDT<4:0>) is modified giving a code identifying the active BTI.

The TEST register file is described in Table 5.3.3.

This register file can be used to program TRACO for track emulation. POS, ANG, TRG and HLB are respectively the position, angle (k-parameter), trigger strobe and high/low quality flag for every BTI input. Once the TESTMODE bit is set high, the event loaded in the TEST register file is processed by TRACO starting from the clock cycle

| Address | MSB - LSB |
|---|---|
| 38 | ANG1<1:0>, POS1<5:0> |
| 39 | POS2<1:0>, TRG1, HLB1, ANG1<5:2> |
| 40 | ANG2<3:0>, POS2<5:2> |
| 41 | POS3<3:0>, TRG2, HLB2, ANG2<5:4> |
| 42 | ANG3<5:0>, POS3<5:4> |
| 43 | POS4<5:0>, TRG3, HLB3 |
| 44 | TRG4, HLB4, ANG4<5:0> |
| 45 | ANG9<1:0>, POS9<5:0> |
| 46 | POS10<1:0>, TRG9, HLB9, ANG9<5:2> |
| 47 | ANG10<3:0>, POS10<5:2> |
| 48 | POS11<3:0>, TRG10, HLB10, ANG10<5:4> |
| 49 | ANG11<5:0>, POS11<5:4> |
| 50 | POS12<5:0>, TRG11, HLB11 |
| 51 | TRG12, HLB12, ANG12<5:0> |
| 52 | PRVMSK<1:0>, PRVDT<5:0> |
| 53 | PHI1<5:0>, PRVMSK<3:2> |
| 54 | DPHI1<1:0>, PHI1<11:6> |
| 55 | DPHI1<9:2> |
| 56 | PHI2<2:0>, MSK1<2:0>, OVL1, FS1 |
| 57 | PHI2<10:3> |
| 58 | DPHI2<6:0>, PHI2<11> |
| 59 | MSK2<2:0>, OVL2, FS2, DPHI2<9:7> |

Tab 5.3.4: SNAP register file

right after the STARTTEST bit is set high. Only events with BTI triggering at the same clock cycle can be simulated.

The SNAP register file is described in Table 5.3.4.

The SNAP resister file can be cleared using the SNPRSTB reset line. As soon as a trigger is generated by TRACO, matching the selection criteria defined by the SNAPCOR parameter, the event is stored in the SNAP registers. The parameters stored are: the track impact parameters and the quality sent by the Inner (1 to 4) and the Outer (9 to 12) BTI, the generated preview data (PRVDT and PRVMSK) and the full information trigger data (PHI, DPHI, FS, OVL and MSK). While only the first track choice is stored for the preview bus, the full information is stored twice, one for each track choice.

### 5.4 JTAG interface

The JTAG port is available for interconnection testing and for TRACO registers programming. The implemented instructions are the mandatory Extest, Bypass and Sample, and the dedicated Config, Test, Snap and Debug as described in Table 5.4.1.

The first one (Extest) is used for PCB testing and in general for system interconnect verification. This function allows writing in all chip outputs a value and to verify that the same pattern can be received at the inputs of downstream connected devices.

The bypass instruction is used to skip a device in the JTAG chain.

Sample instruction allows reading TRACO periphery without interfering with chip operation. Dedicated instructions are used to access Configuration, Test and Snap register files.

| Instruction | Name | Description |
|---|---|---|
| 0 | EXTEST | Boundary scan test |
| 1 | - | - |
| 2 | SAMPLE | Chip boundary sampling |
| 3 | - | - |
| 4 | - | - |
| 5 | - | - |
| 6 | - | - |
| 7 | CONFIG | Configuration register file |
| 8 | TEST | Test register file |
| 9 | SNAP | Snap register file |
| 10 | DEBUG | Pipeline intermediate access |
| 11 | - | - |
| 12 | - | - |
| 13 | - | - |
| 14 | - | - |
| 15 | BYPASS | Chip bypassing |

Tab 5.4.1: JTAG instruction set.

Using the Boundary Scan register TRACO inputs can be set (EXTEST) and outputs can be latched (SAMPLE, EXTEST) and shifted out through the JTAG serial chain (MSB first). The BSC register is described in Figure 5.4.2.

| MSB output – LSB input | Description |
|---|---|
| TRG1, HLB1, AP1<5:0> | BTI input |
| TRG2, HLB2, AP2<5:0> | BTI input |
| TRG3, HLB3, AP3<5:0> | BTI input |
| TRG4, HLB4, AP4<5:0> | BTI input |
| TRG5, HLB5, AP5<5:0> | BTI input |
| TRG6, HLB6, AP6<5:0> | BTI input |
| TRG7, HLB7, AP7<5:0> | BTI input |
| TRG8, HLB8, AP8<5:0> | BTI input |
| TRG9, HLB9, AP9<5:0> | BTI input |
| TRG10, HLB10, AP10<5:0> | BTI input |
| TRG11, HLB11, AP11<5:0> | BTI input |
| TRG12, HLB12, AP12<5:0> | BTI input |
| TRG13, HLB13, AP13<5:0> | BTI input |
| TRG14, HLB14, AP14<5:0> | BTI input |
| TRG15, HLB15, AP15<5:0> | BTI input |
| TRG16, HLB16, AP16<5:0> | BTI input |
| SELECT | TRACO select / PINT strobe |
| POSTSEL | TRACO post-select / PINT r/w |
| THETA | Theta view trigger |
| SEQRST, SEQTST, SEQADV | Emulation sequence controls |
| PRGB | PINT enable |
| ORHL,OLHL, IRHL, ILHL | HLB signals of neighbouring BTIs |
| PHIR<11:0> | TRACO trigger bus |
| DPHI<9:0> | TRACO trigger bus |
| MSK<2:0>, OVLP, FTSTB | TRACO trigger bus |
| DT<7:6>, DT<0:5> | PINT input bus |
| PRVHL, PRVIO, PRV<0:5> | Preview output bus |
| PRVOEb | Preview output enable |
| PRVFSOEb, PRVFS | Preview FTSTB and enable |
| PRVCOROEb, PRVCOR | Preview CORR and enable |
| BTIOEb, BTISTB | BTI strobe and enable |

Tab 5.4.2: Boundary Scan register.

## 5.5 Parallel interface

The TRACO registers can be programmed very efficiently through a parallel interface. This port is controlled by three input lines: PRGB, SELECT (strobe) and POSTSEL (r/w). The I/O data bus uses the same set of pins as the preview trigger bus. As shown in Fig.5.5.1 a low level on PRGB turns on the interface and prevents any trigger data to be generated.

In order to ensure a correct operation of the parallel interface the SELECT input must be inactive (low) when the PRGB is pulled low.

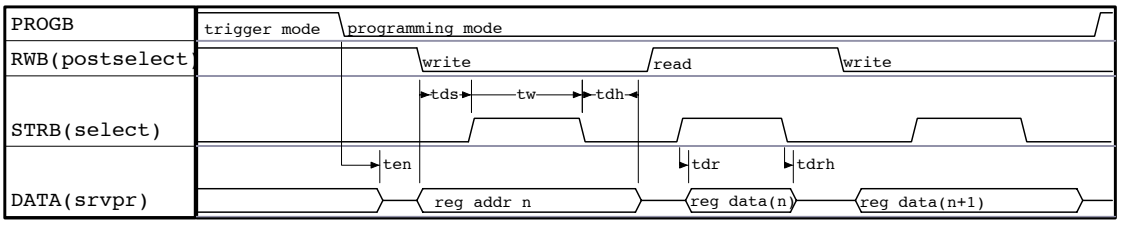



Fig. 5.5.1: Parallel Interface timing.

The internal registers can be accessed randomly or sequentially. After PRGB is pulled low the first input word loaded (on the rising edge of SELECT) is the address pointer and the second one is the value to be loaded. The line POSTSEL is used to chose between Read (1) and Write (0) operation. If PRGB is kept low the address pointer is self-incremented on the falling edge of SELECT and other data can be read or written into the next registers. When reading a location the TRACO output bus is enabled by the SELECT line itself. When PRGB goes high the address pointer is cleared.

The only way to access TRACO look-up tables is by means of this interface.

### 5.6 Operating instructions

TRACO operations start at power on with a hardware reset command, executed pulling low RESETB. While clock is running, the synchronous reset command SRESETB can be used to clear the internal registers with the exception of the CONFIG register file. A dedicated synchronous reset (SNPRSTB) is provided to clear only the SNAP register file without interfering with the triggering function. The TRACO output is meaningless for the first 6 CLOCK cycles after a hardware or software reset. After chip configuration

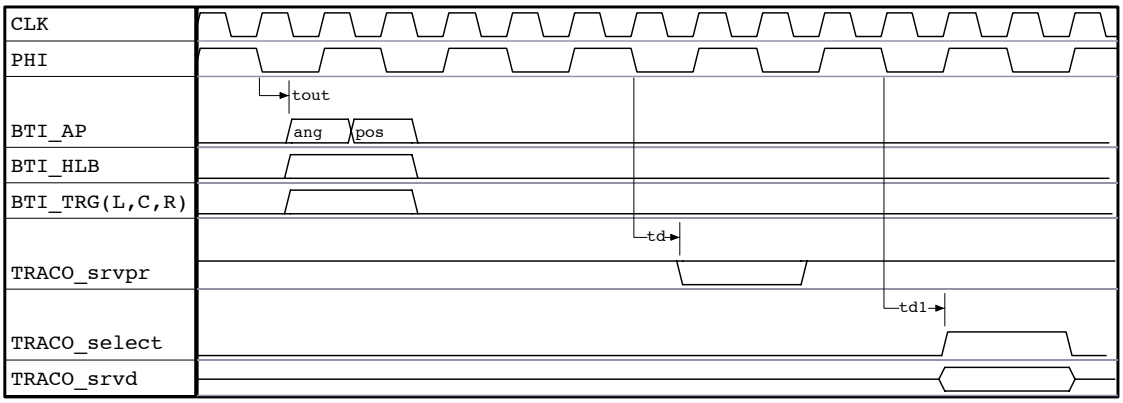



Fig. 5.6.1: TRACO timing.

PRGB must be left high in order to enable the trigger data bus.

The angle/position values provided by BTIs are sampled at the rising/falling edge of CLOCK respectively, BTI trigger strobes and quality bits are sampled on the rising edge while THETA trigger input is sampled on the falling edge (see the timing diagram of Fig.5.6.1). During normal trigger operation TESTMODE, STARTTEST and PRVSIGNMUX must be set to 0.

Each BTI input can be enabled setting the correspondent bit in the CONFIG register (TRGEN<16:1>); noisy channels can be individually disabled by setting low the correspondent enable bit. RAD parameter must be set according to the radial angle (with respect to the normal direction) that is dependent either on chamber location in the CMS wheel or TRACO position in the chamber. BTIC must be set equal to the ST parameter of connected BTIs.

Two CONFIG parameters are dependent on chamber geometry: DD and IBTIOFF. DD must be approximated (the choice is between 16, 18 and 20) to the ratio between the Superlayer distance (considering the median planes), and the distance between wire planes (current nominal value equal to 13 mm). IBTIOFF is typically set to 0 and is the offset of the inner Superlayer with respect to the outer one. This parameter is summed to all track positions provided by inner BTIs.

Correlation tolerance can be changed setting the parameter PRGCOMP (typical value 2) to the maximum allowed difference between the k-parameter of the correlated track, calculated as the difference between the positions of the two track candidates, and the k-parameter of each candidate.

The trigger output is filtered both in time and angle. The LTS algorithm can be turned on setting high the LTS flag and is effective on the 4 clock cycles before any high quality trigger. An angular cut can be applied to the single and correlated Low quality triggers by means of the KPRGCOMP parameter. All low quality triggers are cut when half the absolute value of the bending angle (DPHI) is higher than KPRGCOM.

### 5.8 Test and debug features

Snap registers, connected either to input BTI busses or to output trigger data busses are provided for online trigger system debugging. The snap registers are activated if a trigger is generated matching the selection criteria set by the parameter SNAPCOR. The relevant event information is stored in the registers for subsequent inspection. The JTAG interface can be used to shift out the snap register data allowing to monitor the trigger activity without any interference.

Another testing facility is the possibility to disconnect by software the TRACO from the BTIs and to use the TEST registers to emulate a programmed event. TESTMODE and STARTTEST are respectively the enable flag and the start bit for track emulator circuitry. When TESTMODE is set to 1 all BTI inputs are disabled and the track emulation logic is enabled; the TEST register file is programmed to produce a given track pattern. The emulation starts when the STARTTEST bit is set to 1.

This capability to simulate real tracks can be used on the field to debug the trigger chain.

In order to monitor the trigger electronics functionality during CMS data taking periods using the on-chamber Test Pulse Generator a dedicated sequencer has been implemented. The lines activating the Test Pulse Sequencer are SEQRST, SEQTST and SEQADV. When SEQTST is activated (high) TRACO sorters are disabled and the selection is forced to the BTI of the inner and outer Superlayers addressed by Test Sequence counter. Only BTI 1 to 4 and 9 to 12 can be selected, since only orthogonal tracks can be generated using the Test Pulse Generator (see the Control Board user manual for full specifications. The Test Sequence counter, that ranges from 0 to 3 cyclically is incremented by a

SEQADV cycle and is cleared activating the SEQRST line. The selection of Inner and Outer BTIs during the Test Sequence operation is described in Table 5.8.1.

| ST counter | Inner | Outer |
|---|---|---|
| 0 | 1 | 9 |
| 1 | 2 | 10 |
| 2 | 3 | 11 |
| 3 | 4 | 12 |

Table 5.8.1: BTI selection in Sequence Test mode.

## Appendix A: TRACO algorithm description

```
Coordinates system for BTI:

    k    = kh * tan(a) + k0  ;track angle
    p    = x / (Vd * tck)    ;track position
    where:
    a    = angle wrt normal (positive anti-clockwise)
    x    = position referred to axis of wires 1-2
    kh   = d * 2 / (tck * Vd)
    d    = distance between wire planes (13mm)
    tck  = clock period (25ns)
    Vd   = drift velocity (50um/ns)
    k0   = 2 * Ld / (Vd * tck)
    Ld   = cell length (20mm)

BTI track data:
       ang    k:  6 bit
       pos    p:  6 bit
       qualityhl: 1 bit
       strobe tg: 1 bit


TRACO operations:

       -------------------\----------------------------------------
      | 05 | 06 | 07 | 08 | 09 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |     Outer SL
       ---------------------\-------------------------------------
                             \_| acal
              xcal            \|
      |------------------------\
                                \
                                 \
                            -------\-----------
                           | 01 | 02 | 03 | 04 |                        Inner SL
                            ---------\---------


                      Fig: BTI indexing


Pipeline description:
----------
1ST STAGE:
----------
translate position values for TRACO:
    xcal(i) = (i+4) * k0 + p(i)
    xcal(o) = (o-4) * k0 + p(o)
    where:
    i       = Inner BTI index 0-3 (see Fig)
    o      = Outer BTI index 4-15 (see Fig)

calculate angle values for TRACO:
    acal(i) = k(i) - k0 - kR
    acal(o) = k(o) - k0 - kR
    where:
    kR     = kh * tan(RAD)   ;5 bit
    RAD     = angle of radial line wrt normal

select first best inner and outer candidates:
calculate:
    bhi     = (min((|acal(i)|,(hl(i)=1)) if (HISM1=0)) or
              (max((|acal(i)|,(hl(i)=1)) if (HISM1=1))
       best inner candidate index for high quality tracks
    bi      = (min((|acal(i)|) if (HISM1=0)) or
              (max((|acal(i)|) if (HISM1=1))
       best inner overall candidate index
    bho     = (min((|acal(o)|,(hl(o)=1)) if (HISM1=0)) or
              (max((|acal(o)|,(hl(o)=1)) if (HISM1=1))
       best outer candidate index for high quality tracks
    bo      = (min((|acal(o)|) if (HISM1=0)) or
              (max((|acal(o)|) if (HISM1=1))
       best outer overall candidate index
then select:
    bacali1,bxcali1,bhli1,btgi1  =  ((acal(bhi),xcal(bhi),hl(bhi),tg(bhi))          if
(HTPRF1=1) or
                                    ((acal(bi),xcal(bi),hl(bi),tg(bi)) if (HTPRF1=0)
    bacalo1,bxcalo1,bhlo1,btgo1  =  ((acal(bho),xcal(bho),hl(bho),tg(bho))          if
(HTPRF1=1) or
                                    ((acal(bo),xcal(bo),hl(bo),tg(bo)) if (HTPRF1=0)
```

```
----------
2ND STAGE:
----------
calculate position and angle of first correlated track candidate:
    xcor1    = (bxcali1 + bxcalo1)/2
    acor1    = bxcali1 - bxcalo1 + 512

translate angle coordinates of first best candidates
    aical1   = DD/2 * (bacali1 + kR) + 512
    aocal1   = DD/2 * (bacalo1 + kR) + 512
    where:
    DD       = D/d   ;programmable to 16, 18 or 20
    D        = distance between SuperLayer centers

set correlation flag:
    corr1    = (|acor1 -aical1|/16 <= PRGCOM1) and (|acor1 -aocal1|/16 <= PRGCOM1)
    where:
    PRGCOM1  = alignment tolerance for correlated track segments
                     ;programmable in the range 0-3

first track selection:
    ang1,pos1 are selected between:
                                    acor1,xcor1   (csel1 = 1)
                                    aical1,bxcali1(isel1 = 1)
                                    aocal1,bxcalo1(osel1 = 1)
    according to the following table.
```

| | INPUTS | | | | | | | | | OUTPUTS | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | corr1 | btgi1 | bhli1 | btgo1 | bhlo1 | trge1 | HTMSK1 | LTMSK1 | SLMSK1 | ISEL1 | OSEL1 | CSEL1 | QCODE1 | |
| 1 | 1 | 1 | 1 | 1 | 1 | x | x | x | x | 0 | 0 | 1 | 110 | Corr HH |
| 2 | 1 | 1 | 0 | 1 | 1 | x | x | x | x | 0 | 0 | 1 | 101 | Corr HL |
| 3 | 1 | 1 | 1 | 1 | 0 | x | x | x | x | 0 | 0 | 1 | 101 | " |
| 4 | 1 | 1 | 0 | 1 | 0 | x | x | x | x | 0 | 0 | 1 | 100 | Corr LL |
| 5 | 0 | 1 | 1 | 1 | 1 | x | x | x | 0 | 1 | 0 | 0 | 010 | H Inner |
| 6 | 0 | 1 | 1 | x | 0 | x | 0 | x | x | 1 | 0 | 0 | 010 | " |
| 7 | 0 | 1 | 1 | x | 0 | 1 | 1 | x | x | 1 | 0 | 0 | 010 | " |
| 8 | 0 | 1 | 1 | 1 | 1 | x | x | x | 1 | 0 | 1 | 0 | 011 | H Outer |
| 9 | 0 | x | 0 | 1 | 1 | x | 0 | x | x | 0 | 1 | 0 | 011 | " |
| 10 | 0 | x | 0 | 1 | 1 | 1 | 1 | x | x | 0 | 1 | 0 | 011 | " |
| 11 | 0 | 1 | 0 | 1 | 0 | 1 | x | 0 | 0 | 1 | 0 | 0 | 000 | L Inner |
| 12 | 0 | 1 | 0 | 0 | x | 1 | x | 0 | x | 1 | 0 | 0 | 000 | " |
| 13 | 0 | 1 | 0 | 1 | 0 | 1 | x | 0 | 1 | 0 | 1 | 0 | 001 | L Outer |
| 14 | 0 | 0 | x | 1 | 0 | 1 | x | 0 | x | 0 | 1 | 0 | 001 | " |
| 15 | 0 | 1 | 1 | x | x | 0 | 1 | x | x | 0 | 0 | 0 | 111 | Null |
| 16 | 0 | x | x | 1 | 1 | 0 | 1 | x | x | 0 | 0 | 0 | 111 | " |
| 17 | 0 | x | 0 | x | 0 | x | x | 1 | x | 0 | 0 | 0 | 111 | " |
| 18 | 0 | x | 0 | x | 0 | 0 | x | 0 | x | 0 | 0 | 0 | 111 | " |
| 19 | 0 | 0 | x | 0 | x | x | x | x | x | 0 | 0 | 0 | 111 | " |

```
     where:
     corr1                          ; correlation flag
     btgi1                          ; inner candidate strobe
     bhli1                          ; inner candidate quality
     btgo1                          ; outer candidate strobe
     bhlo1                          ; outer candidate quality
     trge1 = del(TRGEDEL,EXT) or LTF       ; external validation strobe
          where del(TRGEDEL,EXT)    ; Theta superlayer strobe delayed by TRGEDEL (0
to 3bx)
               LTF                  ; Low Trigger Force flag
     HTMSK1                         ; High Trigger Mask
     LTMSK1                         ; Low Trigger Mask
     SLMSK1                         ; Superlayer Mask
     ISEL1                          ; Inner candidate Select
     OSEL1                          ; Outer candidate Select
     CSEL1                          ; Correlated track Select
     QCODE1                         ; track Quality CODE
     (= correlate flag, trigger flag, layer flag)
      = 1 1 1 - no track output         (default)
      = 1 1 0 - correlated H+H
      = 1 0 1 -      //    H+L or L+H
      = 1 0 0 -      //    L+L
      = 0 1 1 - single Htrg from outer
      = 0 1 0 - single Htrg from inner
      = 0 0 1 - single Ltrg from outer
      = 0 0 0 - single Ltrg from inner

first preview track selection:
    pang1 is selected between:
                                    aical1 (pisel1 = 1)
                                    aocal1 (posel1 = 1)
    according to the following table.
```

| | INPUTS | | | | | | | | | | OUTPUTS | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | corr1 | btgi1 | bhli1 | btgo1 | bhlo1 | trge1 | HTPRF1 | LTMSK1 | SLMSK1 | LTF | pisel1 | posel1 | pcsel1 | phl1 | pio1 | |
| 1 | 1 | 1 | 1 | 1 | 1 | x | 1 | x | 0 | x | 1 | 0 | 1 | 0 | 0 | Corr HH |
| 2 | 1 | 1 | 1 | 1 | 1 | x | 1 | x | 1 | x | 0 | 1 | 1 | 0 | 1 | Corr HH |

| | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 3 | 1 | 1 | x | 1 | x | x | 0 | x | 0 | x | 1 | 0 | 1 | 0 | 0 | Corr HL |
| 4 | 1 | 1 | x | 1 | x | x | 0 | x | 1 | x | 0 | 1 | 1 | 0 | 1 | Corr HL |
| 5 | 1 | 1 | 0 | 1 | 0 | x | 1 | x | 0 | x | 1 | 0 | 1 | 0 | 0 | Corr LL |
| 6 | 1 | 1 | 0 | 1 | 0 | x | 1 | x | 1 | x | 0 | 1 | 1 | 0 | 1 | Corr LL |
| 7 | 0 | 1 | 1 | 1 | x | x | x | x | 0 | x | 1 | 0 | 0 | 0 | 0 | H Inner |
| 8 | 0 | 1 | 1 | x | 0 | x | 0 | x | x | x | 1 | 0 | 0 | 0 | 0 | H Inner |
| 9 | 0 | 1 | x | 1 | 1 | x | x | x | 1 | x | 0 | 1 | 0 | 0 | 1 | H Outer |
| 10 | 0 | x | 0 | 1 | 1 | x | 0 | x | x | x | 0 | 1 | 0 | 0 | 1 | H Outer |
| 11 | 0 | 1 | 0 | 1 | x | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | L Inner |
| 12 | 0 | 1 | 0 | 1 | 0 | 1 | x | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | L Inner |
| 13 | 0 | 1 | 0 | 1 | 0 | x | x | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | L Inner |
| 14 | 0 | 1 | 0 | 1 | x | x | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | L Inner |
| 15 | 0 | 1 | 0 | 0 | x | 1 | x | 0 | x | 0 | 1 | 0 | 0 | 1 | 0 | L Inner |
| 16 | 0 | 1 | x | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | L Outer |
| 17 | 0 | 1 | 0 | 1 | 0 | 1 | x | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | L Outer |
| 18 | 0 | 1 | 0 | 1 | 0 | x | x | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | L Outer |
| 19 | 0 | 1 | x | 1 | 0 | x | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | L Outer |
| 20 | 0 | 0 | x | 1 | 0 | 1 | x | 0 | x | 0 | 0 | 1 | 0 | 1 | 1 | L Outer |
| 21 | 0 | 1 | x | 1 | x | 0 | 0 | 0 | x | 0 | 0 | 0 | 1 | 1 | 1 | Null |
| 22 | 0 | 1 | 0 | 1 | 0 | 0 | x | 0 | x | 0 | 0 | 0 | 1 | 1 | 1 | " |
| 23 | 0 | x | 0 | x | 0 | x | x | 1 | x | x | 0 | 0 | 1 | 1 | 1 | " |
| 24 | 0 | x | 0 | x | 0 | 0 | x | 0 | x | 0 | 0 | 0 | 1 | 1 | 1 | " |
| 25 | 0 | 0 | x | 0 | x | x | x | x | x | x | 0 | 0 | 1 | 1 | 1 | " |

```
     where:
     HTPRF1                          ; High Trigger Preference Mask
     pisel1                          ; Inner candidate Select
     posel1                          ; Outer candidate Select
     pcsel1                          ; Correlated track Select
     phl1                            ; H/L quality
     pio1                            ; Inner/Outer flag
```

select second best inner and outer candidates (first best candidates are not considered):

```
calculate:
    bhi     = (min((|acal(i)|,(hl(i)=1)) if (HISM2=0)) or
              (max((|acal(i)|,(hl(i)=1)) if (HISM2=1))
       best inner candidate index for high quality tracks
    bi      =  (min((|acal(i)|) if (HISM2=0)) or
              (max((|acal(i)|) if (HISM2=1))
       best inner overall candidate index
    bho     = (min((|acal(o)|,(hl(o)=1)) if (HISM2=0)) or
              (max((|acal(o)|,(hl(o)=1)) if (HISM2=1))
       best outer candidate index for high quality tracks
    bo      =  (min((|acal(o)|) if (HISM2=0)) or
              (max((|acal(o)|) if (HISM2=1))
       best outer overall candidate index
then select:
    bacali2,bxcali2,bhli2,btgi2   =  ((acal(bhi),xcal(bhi),hl(bhi),tg(bhi))          if
(HTPRF2=1) or
                                     ((acal(bi),xcal(bi),hl(bi),tg(bi)) if (HTPRF2=0)
    bacalo2,bxcalo2,bhlo2,btgo2   =  ((acal(bho),xcal(bho),hl(bho),tg(bho))          if
(HTPRF2=1) or
                                     ((acal(bo),xcal(bo),hl(bo),tg(bo)) if (HTPRF2=0)

----------
3RD STAGE:
----------
calculate chamber coordinates of best track:
    phi = PHILUT(ang*)
    phir = PHIRLUT(pos*)
where PHILUT and PHIRLUT are look-up tables.
PHILUT and PHIRLUT are common for first and second best tracks; second best tracks
(coming from
same stage but previous cycle) are suppressed in case of overlap with a first best
candidate.

calculate position and angle of correlated second track candidate:
    xcor2    = (bxcali2 + bxcalo2)/2
    acor2    = bxcali2 - bxcalo2 + 512

translate angle coordinates of second best candidates
    aical2   = DD/2 * (bacali2 + kR) + 512
    aocal2   = DD/2 * (bacalo2 + kR) + 512
    where:
    DD      = D/d     ;programmable to 16, 18 or 20
    D       = distance between SuperLayer centers

set correlation flag:
    corr2    = (|acor2 -aical2|/16 <= PRGCOM2) and (|acor2 -aocal2|/16 <= PRGCOM2)
    where:
    PRGCOM2  = alignment tolerance for correlated track segments
                     ;programmable in the range 0-3

second track selection:
    ang2,pos2 are selected between:
                                     acor2,xcor2    (csel2 = 1)
                                     aical2,bxcali2 (isel2 = 1)
```

aocal2,bxcalo2 (osel2 = 1)

according to the following table.

| | INPUTS | | | | | | | | | OUTPUTS | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | corr2 | btgi2 | bhli2 | btgo2 | bhlo2 | trge2 | HTMSK2 | LTMSK2 | SLMSK2 | ISEL2 | OSEL2 | CSEL2 | QCODE2 | |
| 1 | 1 | 1 | 1 | 1 | 1 | x | x | x | x | 0 | 0 | 1 | 110 | Corr HH |
| 2 | 1 | 1 | 0 | 1 | 1 | x | x | x | x | 0 | 0 | 1 | 101 | Corr HL |
| 3 | 1 | 1 | 1 | 1 | 0 | x | x | x | x | 0 | 0 | 1 | 101 | " |
| 4 | 1 | 1 | 0 | 1 | 0 | x | x | x | x | 0 | 0 | 1 | 100 | Corr LL |
| 5 | 0 | 1 | 1 | 1 | 1 | x | x | x | 0 | 1 | 0 | 0 | 010 | H Inner |
| 6 | 0 | 1 | 1 | x | 0 | x | 0 | x | x | 1 | 0 | 0 | 010 | " |
| 7 | 0 | 1 | 1 | x | 0 | 1 | 1 | x | x | 1 | 0 | 0 | 010 | " |
| 8 | 0 | 1 | 1 | 1 | 1 | x | x | x | 1 | 0 | 1 | 0 | 011 | H Outer |
| 9 | 0 | x | 0 | 1 | 1 | x | 0 | x | x | 0 | 1 | 0 | 011 | " |
| 10 | 0 | x | 0 | 1 | 1 | 1 | 1 | x | x | 0 | 1 | 0 | 011 | " |
| 11 | 0 | 1 | 0 | 1 | 0 | 1 | x | 0 | 0 | 1 | 0 | 0 | 000 | L Inner |
| 12 | 0 | 1 | 0 | 0 | x | 1 | x | 0 | x | 1 | 0 | 0 | 000 | " |
| 13 | 0 | 1 | 0 | 1 | 0 | 1 | x | 0 | 1 | 0 | 1 | 0 | 001 | L Outer |
| 14 | 0 | 0 | x | 1 | 0 | 1 | x | 0 | x | 0 | 1 | 0 | 001 | " |
| 15 | 0 | 1 | 1 | x | x | 0 | 1 | x | x | 0 | 0 | 0 | 111 | Null |
| 16 | 0 | x | x | 1 | 1 | 0 | 1 | x | x | 0 | 0 | 0 | 111 | " |
| 17 | 0 | x | 0 | x | 0 | x | x | 1 | x | 0 | 0 | 0 | 111 | " |
| 18 | 0 | x | 0 | x | 0 | 0 | x | 0 | x | 0 | 0 | 0 | 111 | " |
| 19 | 0 | 0 | x | 0 | x | x | x | x | x | 0 | 0 | 0 | 111 | " |

where:

corr2 ; correlation flag
btgi2 ; inner candidate strobe
bhli2 ; inner candidate quality
btgo2 ; outer candidate strobe
bhlo2 ; outer candidate quality
trge2 = del(TRGEDEL,EXT) or LTF ; external validation strobe
where del(TRGEDEL,EXT) ; Theta superlayer strobe delayed by TRGEDEL (0 to 3bx)
LTF ; Low Trigger Force flag
HTMSK2 ; High Trigger Mask
LTMSK2 ; Low Trigger Mask
SLMSK2 ; Superlayer Mask
ISEL2 ; Inner candidate Select
OSEL2 ; Outer candidate Select
CSEL2 ; Correlated track Select
QCODE2 ; track Quality CODE

second preview track selection:

pang2 is selected between:

aical2 (pisel2 = 1)
aocal2 (posel2 = 1)

according to the following table.

| | INPUTS | | | | | | | | | | OUTPUTS | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | corr2 | btgi2 | bhli2 | btgo2 | bhlo2 | trge2 | HTPRF2 | LTMSK2 | SLMSK2 | LTF | pisel2 | posel2 | pcsel2 | phl2 | pio2 | |
| 1 | 1 | 1 | 1 | 1 | 1 | x | 1 | x | 0 | x | 1 | 0 | 1 | 0 | 0 | Corr HH |
| 2 | 1 | 1 | 1 | 1 | 1 | x | 1 | x | 1 | x | 0 | 1 | 1 | 0 | 1 | Corr HH |
| 3 | 1 | 1 | x | 1 | x | x | 0 | x | 0 | x | 1 | 0 | 1 | 0 | 0 | Corr HL |
| 4 | 1 | 1 | x | 1 | x | x | 0 | x | 1 | x | 0 | 1 | 1 | 0 | 1 | Corr HL |
| 5 | 1 | 1 | 0 | 1 | 0 | x | 1 | x | 0 | x | 1 | 0 | 1 | 0 | 0 | Corr LL |
| 6 | 1 | 1 | 0 | 1 | 0 | x | 1 | x | 1 | x | 0 | 1 | 1 | 0 | 1 | Corr LL |
| 7 | 0 | 1 | 1 | 1 | x | x | x | x | 0 | x | 1 | 0 | 0 | 0 | 0 | H Inner |
| 8 | 0 | 1 | 1 | x | 0 | x | 0 | x | x | x | 1 | 0 | 0 | 0 | 0 | H Inner |
| 9 | 0 | 1 | x | 1 | 1 | x | x | x | 1 | x | 0 | 1 | 0 | 0 | 1 | H Outer |
| 10 | 0 | x | 0 | 1 | 1 | x | 0 | x | x | x | 0 | 1 | 0 | 0 | 1 | H Outer |
| 11 | 0 | 1 | 0 | 1 | x | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | L Inner |
| 12 | 0 | 1 | 0 | 1 | 0 | 1 | x | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | L Inner |
| 13 | 0 | 1 | 0 | 1 | 0 | x | x | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | L Inner |
| 14 | 0 | 1 | 0 | 1 | x | x | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | L Inner |
| 15 | 0 | 1 | 0 | 0 | x | 1 | x | 0 | x | 0 | 1 | 0 | 0 | 1 | 0 | L Inner |
| 16 | 0 | 1 | x | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | L Outer |
| 17 | 0 | 1 | 0 | 1 | 0 | 1 | x | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | L Outer |
| 18 | 0 | 1 | 0 | 1 | 0 | x | x | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | L Outer |
| 19 | 0 | 1 | x | 1 | 0 | x | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | L Outer |
| 20 | 0 | 0 | x | 1 | 0 | 1 | x | 0 | x | 0 | 0 | 1 | 0 | 1 | 1 | L Outer |
| 21 | 0 | 1 | x | 1 | x | 0 | 0 | 0 | x | 0 | 0 | 0 | 1 | 1 | 1 | Null |
| 22 | 0 | 1 | 0 | 1 | 0 | 0 | x | 0 | x | 0 | 0 | 0 | 1 | 1 | 1 | " |
| 23 | 0 | x | 0 | x | 0 | x | x | 1 | x | x | 0 | 0 | 1 | 1 | 1 | " |
| 24 | 0 | x | 0 | x | 0 | 0 | x | 0 | x | 0 | 0 | 0 | 1 | 1 | 1 | " |
| 25 | 0 | 0 | x | 0 | x | x | x | x | x | x | 0 | 0 | 1 | 1 | 1 | " |

where:

HTPRF2 ; High Trigger Preference Mask
pisel2 ; Inner candidate Select
posel2 ; Outer candidate Select
pcsel2 ; Correlated track Select
phl2 ; H/L quality
pio2 ; Inner/Outer flag

---
4TH STAGE:
---

calculates bending angle

dphi = phir - phi

```
set bending angle enable
    dphien = (dphi < KPRGCOM)

set LTS filter enable
    ltsen =  (no HTRG for next 4 cycles) and (LTS=1) or (LTS=0)
being the TRACO pipeline 4 cycles long it is possible to look for HTRG 4 cycles in
the "future"

----------
5TH STAGE:
----------

track output
    trk(phir,dphi,qcode,I/II,ovlp) if (dphien = 1) and (ltsen = 1) and (SEL = 1)
    else trk("0111111111","011111111111","111","1","1")
where
    phir is the radial angle (10 signed bits)
    dphi is the bending angle (12 signed bits)
    qcode is the quality code (3 bits)
    I/II is the first(1)/second(0) track flag
    ovlp is the second track suppression flag









calculate values for TRACO X-position;
    xcal  = (xi+xo)/2 = [posi+poso+(in+on+4)*BTIC]/2
    xical = xi = (in+4)*BTIC+posi
    xocal = xo = on*BTIC+poso

calculate values for TRACO K-angle;
    acal  = xi+offset-xo = [(4+in)*BTIC+posi+512]-[on*BTIC+poso]
    aical = Dd/2*(ki-BTIC) + offset
    aocal = Dd/2*(ko-BTIC) + offset
obs:the 3 angles are computed in normal and must be correct to radial
    coordinates so need to subtrate RAD

calculate values for preview output bus (6bits):
prv =  "best ki or ko" - BTIC - RAD

--------------------------------------------------------------------------------
```

## Appendix B: TRACO simulation event database

```
Track simulation database files can be found in the fast_asic directory inside TRACO
directory and are called traco_x.dtb

DATA BASE input format for simulation:
    ANGPOS with indice (from 0 to 15) is a 8 + 8 bit word formed with
            ANGi - is the 6 bit K value from BTI n-th  plus
            POSi - is the 6 bit X value from BTI n-th

    TRG     trigger strobes for each BTI, grouped in one unique word
            tgr[16:1] = {tgo12,tgo11,tgo10,tgo9,tgo8,tgo7,tgo6,tgo5,
                         tgo4,tgo3,tgo2,tgo1,tgi4,tgi3,tgi2,tgi1}
    HLB     hlb-quality bit for each BTI, grouped in one unique word
            hlb[16:1] = {hlo12,hlo11,hlo10,hlo9,hlo8,hlo7,hlo6,hlo5,
                         hlo4,hlo3,hlo2,hlo1,hli4,hli3,hli2,hli1}
    MASK    ={fhism,fhtprf,fhtmsk,fltmsk,fslmsk,fprgcomp[1],fprgcomp[0],
              shism,shtprf,shtmsk,sltmsk,sslmsk,sprgcomp[1],sprgcomp[0],
              ltf,lts}

    MASK flags:(different masks for first-"f" and second-"s" choice)
    hism=1 search for higger radial angles, =0 search for lower radial angle
    htprf=1 high trg preference sorting, =0 disable high trg preference sorting
-------------------------------------------------------------------------------
  htmsk= high trg mask, =0 always accept , =1 depends of trg0
    ltmsk= low trg enable,  =0 depends of teta ,=1 never accept
    slmsk= super layer mask , =0 priority to inner SL, =1 prior. to outer SL
    prgcom = 00 , acceptance of acomparator =+/- 0
    prgcom = 01 , acceptance of acomparator =+/- 1
    prgcom = 10 , acceptance of acomparator =+/- 2
    prgcom = 11 , acceptance of acomparator =+/- 3
    ltf= low trigger force, all low trigger pass without trigger teta confirm.
    lts= supress low trigger (type LL, Li, Lo) in the 4 BX cycles before a H quality
-------------------------------------------------------------------------------
| ltf  |  ltmsk  |                     action                                |
-------------------------------------------------------------------------------
|  0   |    0    | depents of trigger teta signal distributed by the server |
|  1   |    0    | always accept the low trigger                            |
|  0   |    1    | never accept the low trigger                             |
|  1   |    1    | never accept the low trigger                             |
-------------------------------------------------------------------------------

    TANG    K value of the "real" track
    TPOS    X value of the "real" track
    Thet    trigger teta information corresponds to axial direction (2 bits)
            bit[0] gives the quality of trigger teta (=1 High/=0 Low)
            bit[1] gives the existence of  trigger teta
    {ilhl,irhl,olhl,orhl}           //four H/L bits from neigbour BTIs
    NBX     bunch crossing number (8bits)
    WORD    ={Thet[1],Thet[0],nc,nc,ilhl,irhl,olhl,orhl,NBX[7:0]}
    NEV     event number (16bits)
    BTIC    step of measurement use in BTI deppending from drift veloc. (6bits)
    RAD     local radial parameter for each correlator (5bits)
            (to correct the normal angle to radial angle)
    Dd      ratio between distance inter-SuperLayers and inter-wires (5bits)

three lines like this for each bunch crossing with at least one candidate :

-------------------------------------------------------------------------------
ANGPOSi01 ANGPOSi02 ANGPOSo03 ANGPOSi04 ANGPOSo01 ANGPOSo02 ANGPOSo03 ANGPOSo04
-------------------------------------------------------------------------------
ANGPOSo05 ANGPOSo06 ANGPOSo07 ANGPOSo08 ANGPOSo09 ANGPOSo10 ANGPOSo11 ANGPOSo12
-------------------------------------------------------------------------------
 TRG        HLB       MASK      TANG      TPOS      WORD      NEV   BTIC+RAD+Dd
-------------------------------------------------------------------------------
  1          2         3         4         5         6         7         8
-------------------------------------------------------------------------------
TRACO device Input/Output signals

input ck;                           //40 Mhz clock input
input [5:0] dti1,dti2,dti3,dti4;    //data bus from four inner BTIs
input hli1,hli2,hli3,hli4;          //High/Low from four inner BTIs
input tgi1,tgi2,tgi3,tgi4;          //trigger from four inner BTIs
input [5:0] dto1,dto2,dto3,dto4,dto5,dto6,dto7,dto8,dto9,dto10,dto11,dto12;
            //data bus from tweelve outer BTIs
input hlo1,hlo2,hlo3,hlo4,hlo5,hlo6,hlo7,hlo8,hlo9,hlo10,hlo11,hlo12;
            //High/Low from tweelve outer inner BTIs
input tgo1,tgo2,tgo3,tgo4,tgo5,tgo6,tgo7,tgo8,tgo9,tgo10,tgo11,tgo12;
            //trigger from tweelve outer inner BTIs
input ilhl,irhl,olhl,orhl;          //four H/L bits from neigbour BTIs
```

```
input trga;                          //trig from teta view already filtered
                                       (high/low)

output [11:0] phir;                  //angle radial (12 bits)
output [9:0] dphi;                   //delta ang radial (10 bits)
output [2:0] srvmsk;                 //type mask to server
output ovlp,ftstb;                   //other masks to server
output [5:0] pang;                   //preview angle(signal+5bits)
output phl, pio, pfs, pcor;          //preview flags

The output bus is 27 bits  grouped as:
output [26:0]  {phir[11:0],dphi[9:0],srvmux[4:0]}

where srvmux[4:0] = (if prvsignmux=1) {srvmsk[2:0],ovlp,ftstb}
                  = (if prvsignmux=0) {btinumb[3:0],trknull}


the srvmsk are the concatenation of the following three flags coded as:
cflag, tflag, lflag = correlate flag, trigger flag, layer flag
      = 1 1 1 - no track output                              (default = 111)
      = 1 1 0 - correlated H+H
      = 1 0 1 -      //    H+L or L+H
      = 1 0 0 -      //    L+L
      = 0 1 1 - single Htrg from outer
      = 0 1 0 - single Htrg from inner
      = 0 0 1 - single Ltrg from outer
      = 0 0 0 - single Ltrg from inner
other masks to server are:
    ovlp = 1 outputs one first track but exist second track from previous BX
    ftstb = 1 first track choice, =0 means second track choice or nothing

the preview output masks:
    phl  = 0 means high trigger, =1 means low trigger          (default = 1)
    pio  = 0 means inner Sl choice, =1 means outer SL choice   (default = 1)
    pfs  = 0 means first track choice, =1 means second track   (default = 1)
    pcor = 0 the candidates correlated successefully           (default = 1)
```

## Appendix C: TRACO Technical Specification

. Operating voltage 3.3V ± 0.3V
. TTL/CMOS compatible inputs
. Operating speed 40MHz (80MHz sampling of BTI bus)
. JTAG interface
. Parallel interface
. Emulation and monitoring features
. Short lead QFP 240 pin package

## SQFP240 pinout

| Pin | Name | Type | Pin | Name | Type |
|---|---|---|---|---|---|
| 1 | Vdd | Core | 38 | Srvpcr | Out 3-State + pullup |
| 2 | VddAC | Periphery AC | 39 | Srvpfs | Out 3-State + pullup |
| 6 | Bti13dt0 | Input + pulldown | 40 | Srvphl | I/O + pullup |
| 7 | Bti13dt1 | Input + pulldown | 41 | Srvpio | I/O + pullup |
| 8 | Bti13dt2 | Input + pulldown | 42 | Srvpr0 | I/O + pullup |
| 9 | Bti13dt3 | Input + pulldown | 43 | Srvpr1 | I/O + pullup |
| 10 | Bti13dt4 | Input + pulldown | 44 | Srvpr2 | I/O + pullup |
| 11 | Bti13dt5 | Input + pulldown | 45 | Srvpr3 | I/O + pullup |
| 12 | Bti13trg | Input + pulldown | 46 | Srvpr4 | I/O + pullup |
| 13 | Bti13hlb | Input + pulldown | 47 | Srvpr5 | I/O + pullup |
| 14 | Bti14dt0 | Input + pulldown | 48 | Tck | Input Schmitt + pulldown |
| 15 | Bti14dt1 | Input + pulldown | 49 | Tms | Input Schmitt + pullup |
| 16 | Bti14dt2 | Input + pulldown | 50 | Tdi | Input Schmitt + pullup |
| 17 | Bti14dt3 | Input + pulldown | 51 | Tdo | Out 3-State + pullup |
| 18 | Bti14dt4 | Input + pulldown | 52 | Bist_test | Input Schmitt + pulldown |
| 19 | Bti14dt5 | Input + pulldown | 53 | Seqrst | Input Schmitt + pulldown |
| 20 | Bti14trg | Input + pulldown | 54 | Seqtst | Input Schmitt + pulldown |
| 21 | Bti14hlb | Input + pulldown | 55 | Seqadv | Input Schmitt + pulldown |
| 22 | Bti15dt0 | Input + pulldown | 59 | VssAC | Periphery AC |
| 23 | Bti15dt1 | Input + pulldown | 60 | VssDC | Periphery DC |
| 24 | Bti15dt2 | Input + pulldown | 61 | Vss | Core |
| 25 | Bti15dt3 | Input + pulldown | 62 | VssAC | Periphery AC |
| 26 | Bti15dt4 | Input + pulldown | 63 | VddAC | Periphery AC |
| 27 | Bti15dt5 | Input + pulldown | 64 | Bti4hlb | I/O + pulldown |
| 28 | Bti15trg | Input + pulldown | 65 | Bti4trg | Input + pulldown |
| 29 | Bti15hlb | Input + pulldown | 66 | Bti4dt5 | I/O + pulldown |
| 30 | Bti16dt0 | Input + pulldown | 67 | Bti4dt4 | I/O + pulldown |
| 31 | Bti16dt1 | Input + pulldown | 68 | Bti4dt3 | I/O + pulldown |
| 32 | Bti16dt2 | Input + pulldown | 69 | Bti4dt2 | I/O + pulldown |
| 33 | Bti16dt3 | Input + pulldown | 70 | Bti4dt1 | I/O + pulldown |
| 34 | Bti16dt4 | Input + pulldown | 71 | Bti4dt0 | I/O + pulldown |
| 35 | Bti16dt5 | Input + pulldown | 72 | Bti3hlb | I/O + pulldown |
| 36 | Bti16trg | Input + pulldown | 73 | Bti3trg | Input + pulldown |
| 37 | Bti16hlb | Input + pulldown | 74 | Bti3dt5 | I/O + pulldown |

| Pin | Name | Type | Pin | Name | Type |
|---|---|---|---|---|---|
| 75 | Bti3dt4 | I/O + pulldown | 109 | Srvdt1 | Output 3-State + pullup |
| 76 | Bti3dt3 | I/O + pulldown | 110 | Srvdt2 | Output 3-State + pullup |
| 77 | Bti3dt2 | I/O + pulldown | 111 | Srvdt3 | Output 3-State + pullup |
| 78 | Bti3dt1 | I/O + pulldown | 112 | Srvdt4 | Output 3-State + pullup |
| 79 | Bti3dt0 | I/O + pulldown | 113 | Srvdt5 | Output 3-State + pullup |
| 80 | Bti2hlb | I/O + pulldown | 114 | Srvdt6 | Output 3-State + pullup |
| 81 | Bti2trg | Input + pulldown | 115 | Srvdt7 | Output 3-State + pullup |
| 82 | VssAC | Periphery AC | 116 | Srvdt8 | Output 3-State + pullup |
| 83 | VddAC | Periphery AC | 117 | Srvdt9 | Output 3-State + pullup |
| 84 | Bti2dt5 | I/O + pulldown | 118 | Srvdt10 | Output 3-State + pullup |
| 85 | Bti2dt4 | I/O + pulldown | 119 | VddAC | Periphery AC |
| 86 | Bti2dt3 | I/O + pulldown | 120 | VddDC | Periphery DC |
| 87 | Bti2dt2 | I/O + pulldown | 122 | Vdd | Core |
| 88 | Bti2dt1 | I/O + pulldown | 123 | VddAC | Periphery AC |
| 89 | Bti2dt0 | I/O + pulldown | 127 | VssAC | Periphery AC |
| 90 | Bti1hlb | I/O + pulldown | 128 | Theta | Input Schmitt + pulldown |
| 91 | Bti1trg | Input + pulldown | 129 | Orhl | Input Schmitt + pulldown |
| 92 | Bti1dt5 | I/O + pulldown | 130 | Olhl | Input Schmitt + pulldown |
| 93 | Bti1dt4 | I/O + pulldown | 131 | Irhl | Input Schmitt + pulldown |
| 94 | Bti1dt3 | I/O + pulldown | 132 | Ilhl | Input Schmitt + pulldown |
| 95 | Bti1dt2 | I/O + pulldown | 133 | Snprstb | Input Schmitt + pullup |
| 96 | Bti1dt1 | I/O + pulldown | 134 | Sresetb | Input Schmitt + pullup |
| 97 | Bti1dt0 | I/O + pulldown | 135 | Resetb | Input Schmitt + pullup |
| 98 | Vss | Core | 136 | Prgb | Input Schmitt + pulldown |
| 99 | Vdd | Core | 137 | Select | Input Schmitt + pulldown |
| 100 | VddDC | Periphery DC | 138 | Postsel | Input Schmitt + pulldown |
| 101 | Vss | Core | 139 | Srvdt11 | Output 3-State + pullup |
| 102 | VssDC | Periphery DC | 140 | Srvdt12 | Output 3-State + pullup |
| 103 | Vss | Core | 141 | Srvdt13 | Output 3-State + pullup |
| 104 | VddDC | Periphery DC | 142 | Srvdt14 | Output 3-State + pullup |
| 105 | Clock | Input Schmitt + pulldown | 143 | VddAC | Periphery AC |
| 106 | VssDC | Periphery DC | 144 | VssAC | Periphery AC |
| 107 | Btistrb | Out 3-State + pullup | 145 | Srvdt15 | Output 3-State + pullup |
| 108 | Srvdt0 | Output 3-State + pullup | 146 | Srvdt16 | Output 3-State + pullup |

| Pin | Name | Type | Pin | Name | Type |
|---|---|---|---|---|---|
| 147 | Srvdt17 | Output 3-State + pullup | 195 | Bti8dt1 | Input + pulldown |
| 148 | Srvdt18 | Output 3-State + pullup | 196 | Bti8dt2 | Input + pulldown |
| 149 | Srvdt19 | Output 3-State + pullup | 197 | Bti8dt3 | Input + pulldown |
| 150 | Srvdt20 | Output 3-State + pullup | 198 | Bti8dt4 | Input + pulldown |
| 151 | Srvdt21 | Output 3-State + pullup | 199 | Bti8dt5 | Input + pulldown |
| 152 | Srvdt22 | Output 3-State + pullup | 200 | Bti8trg | Input + pulldown |
| 153 | VddAC | Periphery AC | 201 | Bti8hlb | Input + pulldown |
| 154 | VssAC | Periphery AC | 202 | Bti9dt0 | Input + pulldown |
| 155 | Srvdt23 | Output 3-State + pullup | 203 | Bti9dt1 | Input + pulldown |
| 156 | Srvdt24 | Output 3-State + pullup | 204 | Bti9dt2 | Input + pulldown |
| 157 | Srvdt25 | Output 3-State + pullup | 205 | Bti9dt3 | Input + pulldown |
| 158 | Srvdt26 | Output 3-State + pullup | 206 | Vss | Core |
| 159 | Vss | Core | 207 | Vdd | Core |
| 160 | Vdd | Core | 208 | Bti9dt4 | I/O + pulldown |
| 161 | Bti5dt0 | Input + pulldown | 209 | Bti9dt5 | I/O + pulldown |
| 162 | Bti5dt1 | Input + pulldown | 210 | Bti9trg | Input + pulldown |
| 163 | Bti5dt2 | Input + pulldown | 211 | Bti9hlb | I/O + pulldown |
| 164 | Bti5dt3 | Input + pulldown | 212 | Bti10dt0 | I/O + pulldown |
| 165 | Bti5dt4 | Input + pulldown | 213 | Bti10dt1 | I/O + pulldown |
| 166 | Bti5dt5 | Input + pulldown | 214 | Bti10dt2 | I/O + pulldown |
| 167 | Bti5trg | Input + pulldown | 215 | Bti10dt3 | I/O + pulldown |
| 168 | Bti5hlb | Input + pulldown | 216 | Bti10dt4 | I/O + pulldown |
| 169 | Bti6dt0 | Input + pulldown | 217 | Bti10dt5 | I/O + pulldown |
| 170 | Bti6dt1 | Input + pulldown | 218 | Bti10trg | Input + pulldown |
| 171 | Bti6dt2 | Input + pulldown | 219 | Bti10hlb | I/O + pulldown |
| 172 | Bti6dt3 | Input + pulldown | 220 | Bti11dt0 | I/O + pulldown |
| 173 | Bti6dt4 | Input + pulldown | 221 | Bti11dt1 | I/O + pulldown |
| 174 | Bti6dt5 | Input + pulldown | 222 | Bti11dt2 | I/O + pulldown |
| 175 | Bti6trg | Input + pulldown | 223 | Bti11dt3 | I/O + pulldown |
| 176 | Bti6hlb | Input + pulldown | 224 | Bti11dt4 | I/O + pulldown |
| 177 | Bti7dt0 | Input + pulldown | 225 | Bti11dt5 | I/O + pulldown |
| 178 | Bti7dt1 | Input + pulldown | 226 | Bti11trg | Input + pulldown |
| 179 | VssAC | Periphery AC | 227 | Bti11hlb | I/O + pulldown |
| 180 | VssDC | Periphery DC | 228 | Bti12dt0 | I/O + pulldown |
| 184 | Vss | Core | 229 | Bti12dt1 | I/O + pulldown |
| 185 | VssAC | Periphery AC | 230 | Bti12dt2 | I/O + pulldown |
| 187 | VddAC | Periphery AC | 231 | Bti12dt3 | I/O + pulldown |
| 188 | Bti7dt2 | Input + pulldown | 232 | Bti12dt4 | I/O + pulldown |
| 189 | Bti7dt3 | Input + pulldown | 233 | Bti12dt5 | I/O + pulldown |
| 190 | Bti7dt4 | Input + pulldown | 234 | Bti12trg | Input + pulldown |
| 191 | Bti7dt5 | Input + pulldown | 235 | Bti12hlb | I/O + pulldown |
| 192 | Bti7trg | Input + pulldown | 236 | VssAC | Periphery AC |
| 193 | Bti7hlb | Input + pulldown | 239 | VddAC | Periphery AC |
| 194 | Bti8dt0 | Input + pulldown | 240 | VddDC | Periphery DC |

## Absolute maximum ratings

| Parameter | Min | Max | Unit | Conditions |
|---|---|---|---|---|
| DC supply voltage | -0.3 | 4.6 | V | |
| DC input diode current | -10 | 10 | mA | |
| DC output diode current | -10 | 10 | mA | |
| Time of otputs shorted | | 5 | s | |
| Storage temperature | -65 | 150 | °C | |
| Ambient free air temperature range | -40 | 85 | °C | Industrial |

## Recommended operating conditions

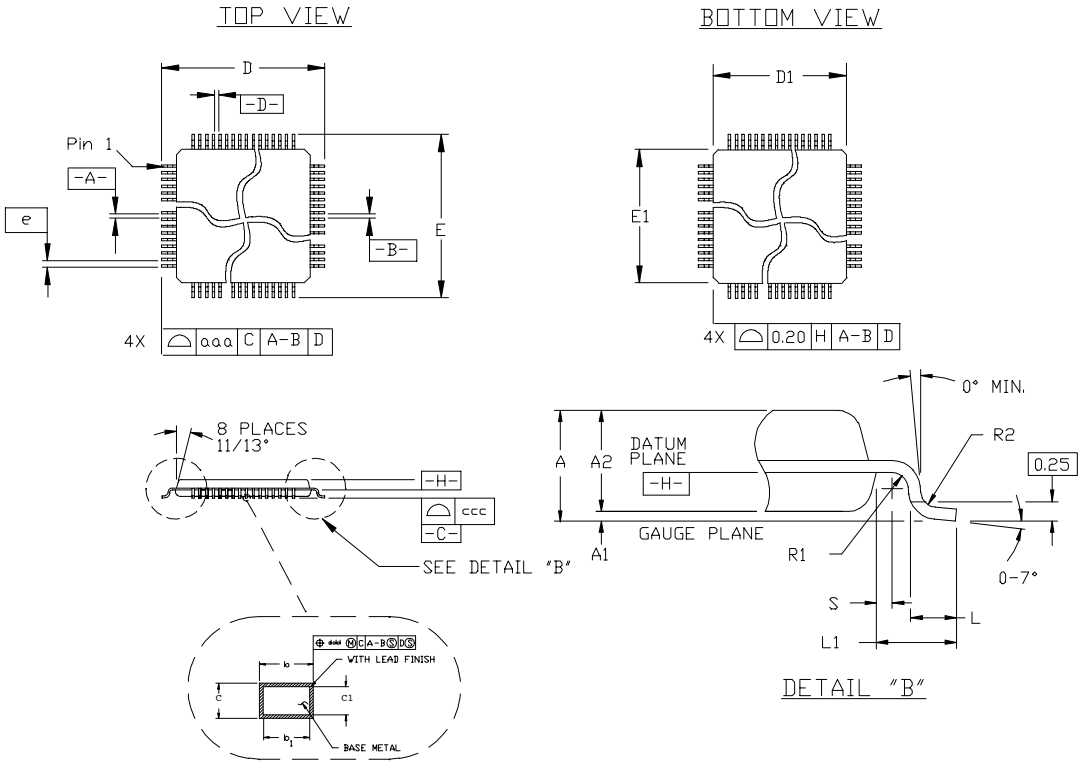
| **Electrical characteristics** | | | | |
|---|---|---|---|---|
| Parameter | Min | Typ | Max | Conditions |
| DC supply voltage | 3.0V | 3.3V | 3.6V | |
| Low level input voltage | -0.3V | | 0.3*Vdd | |
| High level input voltage | 0.7*VDD | | Vdd+0.3V | |
| Low level output v.ge | | | Vss+0.1V | 2.7V IOL=0.3mA CMOS |
| High level output v.ge | Vdd-0.1V | | | 2.7V IOL=0.3mA CMOS |
| Low level output v.ge | | | 0.4V | 2.7V IOL=2 to 8 mA TTL |
| High level output v.ge | 2.4V | | | 2.7V IOL=2 to 8mA TTL |
| **Pullups and pulldowns** | | | | |
| Pullup current | -77µA | | -300µA | @0V worst case |
| Pulldown current | 79µA | | 396µA | @3.3V worst case |
| **AC output characteristics** [2] | | | | |
| Bti_dt_, Bti_hlb, Tdo | 0.168 | 0.095 | 0.052 | ns/pF rise time |
| | 0.188 | 0.106 | 0.058 | ns/pF fall time |
| | | 2mA | | AC Drive current |
| | | 2mA | | DC Drive current |
| Srvp*, Btistrb | 0.085 | 0.048 | 0.026 | ns/pF rise time |
| | 0.094 | 0.053 | 0.029 | ns/pF fall time |
| | | 4mA | | AC Drive current |
| | | 2mA | | DC Drive current |
| Srvdt* | 0.058 | 0.033 | 0.018 | ns/pF rise time |
| | 0.064 | 0.036 | 0.020 | ns/pF fall time |
| | | 6mA | | AC Drive current |
| | | 2mA | | DC Drive current |
| **AC input characteristics** | | | | |
| Input rise time | | | 10ns | CMOS and TTL inputs |
| Input rise time | | | No limit | Schmitt inputs |
| Schmitt input threshold | 1.39V | 1.66V | 1.8V | VT+ |
| " | 0.85V | 1.05V | 1.16V | VT- |
| Schmitt input hysteresis | 0.48V | 0.62V | 0.66V | |

[1] Worst case temperature, voltage and process corners.

[2] Unless otherwise specified VDD=3.3V, T=25°C, typical process, input slope = 1ns.

## Package characteristics

| | | |
|---|---|---|
| **SQFP240** | Thermal resistance | 35°C/W |
| | Lead resistance | 63 - 80 mΩ |
| | Self inductance | 7.7 – 11 nH |
| | Mutual inductance | 5.0 – 7.5 nH |
| | Bulk capacitance | 1.5 – 2.3 pF |
| | Mutual capacitance | 0.7 – 1.0 pF |



Common dimensions (mm) for pin count from 64 to 208:

| Symbol | Min | Nom | Max |
|---|---|---|---|
| c | 0.11 | | 0.23 |
| c1 | 0.11 | 0.15 | 0.19 |
| L | 0.65 | 0.88 | 1.03 |
| L1 | 1.60 REF. | | |
| R2 | 0.13 | | 0.3 |
| R1 | 0.13 | | |
| S | 0.4 | | |
| Tolerances of form and position | | | |
| aaa | | 0.25 | |
| ccc | | | 0.1 |

Common dimensions (mm) for pin count from 240 to 304:

| Symbol | Min | Nom | Max |
|---|---|---|---|
| c | 0.09 | | 0.20 |
| c1 | 0.09 | | 0.16 |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 1.30 REF. | | |
| R2 | 0.08 | | 0.25 |
| R1 | 0.08 | | |
| S | 0.20 | | |
| Tolerances of form and position | | | |
| aaa | | 0.20 | |
| ccc | | | 0.1 |

Dimensions depending from lead count:

| Pin Count | A | A1 | | A2 | | | b | | b1 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | Max | Min | Max | Min | Nom | Max | Min | Max | Min | Nom | Max |
| 44 | 2.70 | 0.25 | 0.50 | 1.80 | 2.00 | 2.20 | 0.29 | 0.45 | 0.29 | 0.35 | 0.41 |
| 52 | 2.45 | 0.00 | 0.25 | 1.80 | 2.00 | 2.20 | 0.34 | 0.50 | 0.34 | 0.40 | 0.46 |
| 64 ♦ | 3.4 | 0.25 | 0.50 | 2.55 | 2.8 | 3.05 | 0.35 | 0.5 | 0.35 | 0.4 | 0.45 |
| 80 ♦ | 3.4 | 0.25 | 0.50 | 2.55 | 2.8 | 3.05 | 0.3 | 0.45 | 0.3 | 0.35 | 0.4 |
| 100 ♦ | 3.4 | 0.25 | 0.50 | 2.55 | 2.8 | 3.05 | 0.22 | 0.38 | 0.22 | 0.3 | 0.33 |
| 120 | 4.10 | 0.25 | 0.50 | 3.20 | 3.40 | 3.60 | 0.29 | 0.45 | 0.29 | 0.35 | 0.41 |
| 128 | 4.10 | 0.25 | 0.50 | 3.20 | 3.40 | 3.60 | 0.29 | 0.45 | 0.29 | 0.35 | 0.41 |
| 144 | 4.10 | 0.25 | 0.50 | 3.20 | 3.40 | 3.60 | 0.29 | 0.45 | 0.29 | 0.35 | 0.41 |
| 160 | 4.10 | 0.25 | 0.50 | 3.20 | 3.40 | 3.60 | 0.29 | 0.45 | 0.29 | 0.35 | 0.41 |
| 208 | 4.10 | 0.25 | 0.50 | 3.20 | 3.40 | 3.60 | 0.17 | 0.27 | 0.17 | 0.20 | 0.23 |
| 240 | 4.10 | 0.25 | 0.50 | 3.20 | 3.40 | 3.60 | 0.17 | 0.27 | 0.17 | 0.20 | 0.23 |
| 256 | 4.10 | 0.25 | 0.50 | 3.20 | 3.40 | 3.60 | 0.13 | 0.23 | 0.13 | 0.16 | 0.19 |
| 304 ♦♦ | 4.50 | 0.25 | 0.50 | 3.60 | 3.80 | 4.00 | 0.17 | 0.27 | 0.17 | 0.20 | 0.23 |

| Pin Count | D BSC | D1 BSC | E BSC | E1 BSC | e BSC | ddd |
|---|---|---|---|---|---|---|
| 44 | 13.20 | 10.00 | 13.20 | 10.00 | 0.8 | 0.2 |
| 52 | 13.20 | 10.00 | 13.20 | 10.00 | 0.65 | 0.13 |
| 64 ♦ | 23.20 | 20.00 | 17.20 | 14.00 | 1.0 | 0.2 |
| 80 ♦ | 23.20 | 20.00 | 17.20 | 14.00 | 0.80 | 0.2 |
| 100 ♦ | 23.20 | 20.00 | 17.20 | 14.00 | 0.65 | 0.12 |
| 120 | 31.20 | 28.00 | 31.20 | 28.00 | 0.80 | 0.2 |
| 128 | 31.20 | 28.00 | 31.20 | 28.00 | 0.80 | 0.2 |
| 144 | 31.20 | 28.00 | 31.20 | 28.00 | 0.65 | 0.12 |
| 160 | 31.20 | 28.00 | 31.20 | 28.00 | 0.65 | 0.12 |
| 208 | 31.20 | 28.00 | 31.20 | 28.00 | 0.50 | 0.10 |
| 240 | 34.60 | 32.00 | 34.60 | 32.00 | 0.50 | 0.10 |
| 256 | 30.60 | 28.00 | 30.60 | 28.00 | 0.40 | 0.10 |
| 304 ♦♦ | 42.60 | 40.00 | 42.60 | 40.00 | 0.50 | 0.10 |

Note:

♦ these packages are rectangular

♦♦ Pin number: 6, 18, 30, 42, 54, 66, 94, 106, 118, 130, 142, 170, 158, 182, 194, 206, 218, 234, 246, 258, 270, 294 must be connected to GND.
Pin number: 7, 19, 31, 43, 55, 67, 95, 107, 119, 131, 143, 159, 171, 195, 207, 219, 235, 247, 259, 271, 295 are interconnected to VCC.

## References

[1] M. De Giorgi et al., Nuclear Instruments and Methods in Physics Research,A398 (1997), 203.
[2] G.M. Dallavalle et al., Proceedings of Fourth Workshop on Electronics for LHC experiments, CERN/LHCC/98-36, 294.
[3] A Kluge and T. Wildsheck, CMS NOTE 1997/091.
A Kluge and T. Wildsheck, CMS NOTE 1997/092.
A Kluge and T. Wildsheck, CMS NOTE 1997/093.
[4] M. De Giorgi et al., CMS TN 95/01